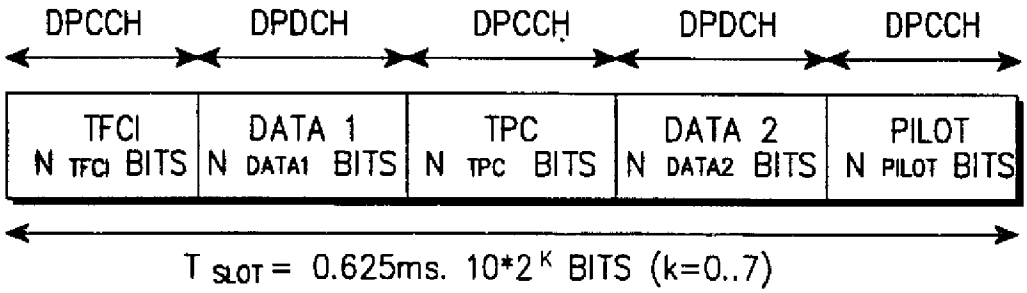

DPCCH
DPDCH
DPCCH
DPDCH
DPCCH
TFCI
N TFCI BITS
DATA 1
N DATA1 BITS
TPC
N TPC BITS
DATA 2
N DATA2 BITS
PILOT
N PILOT BITS
T SLOT = 0.625ms. 10*2 K BITS (k=0..7)

FIG. 2A

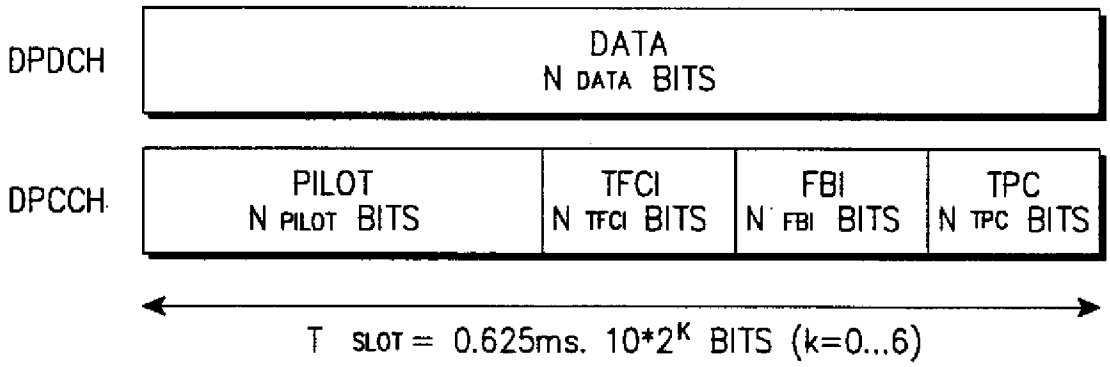

DPDCH
DATA
N DATA BITS
DPCCH
PILOT
N PILOT BITS
TFCI
N TFCI BITS
FBI
N FBI BITS
TPC
N TPC BITS
T SLOT = 0.625ms. 10*2K BITS (k=0...6)

FIG. 2B

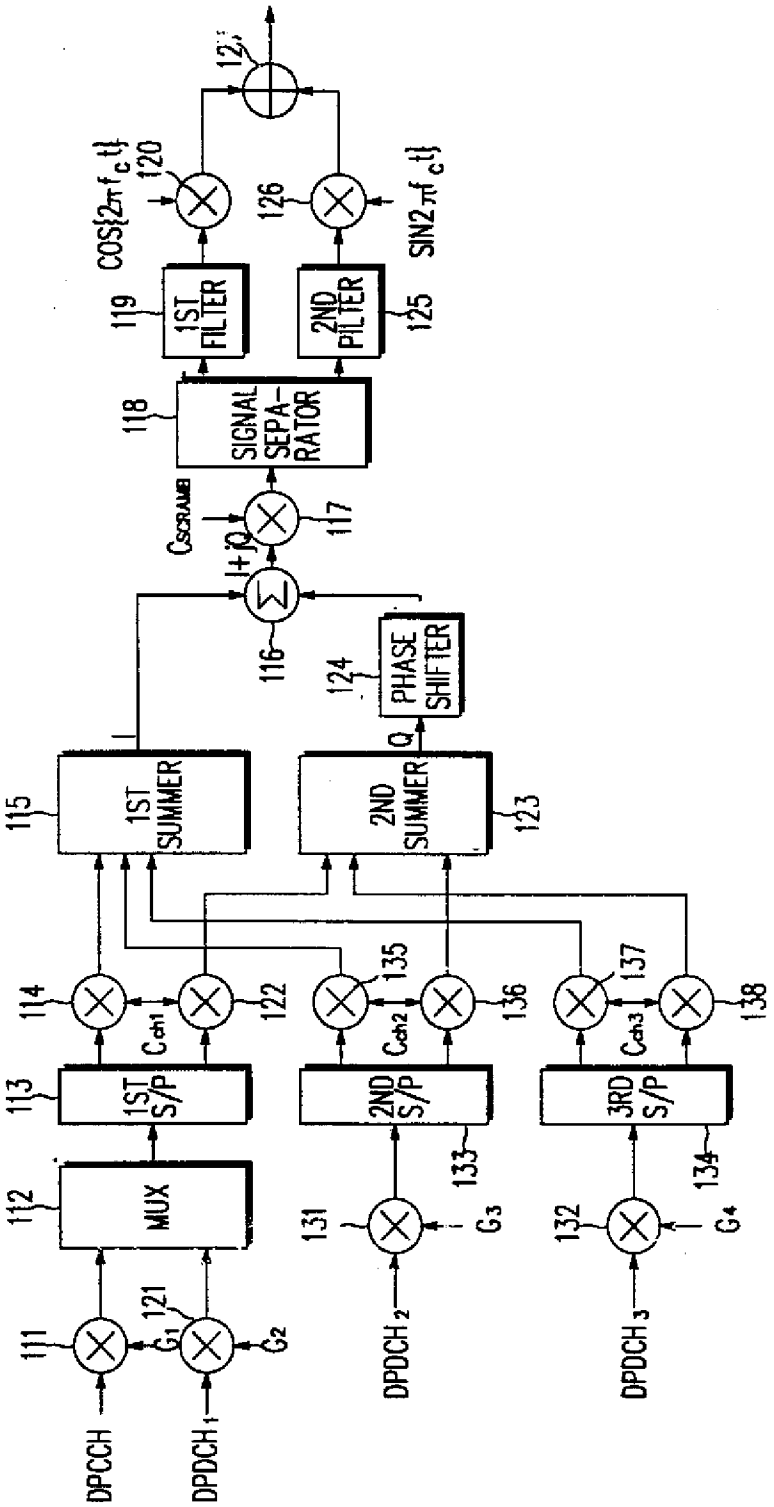

DPCCH
DPDCH1
DPDCH2
DPDCH3
111
121
G1
G2
112
MUX
113
1ST S/P
2ND S/P
3RD S/P
114
122
135
136
137
138
131
132
133
134
G3
G4
Cch1
Cch2
Cch3
115
1ST SUMMER
2ND SUMMER
123
124
PHASE SHIFTER
116
I+jQ
117
CSCRAMBLE
118
SIGNAL SEPA-RATOR
119
1ST FILTER
2ND FILTER
125
120
126
COS{2πfct}
SIN2πfct}
12'

FIG. 3A

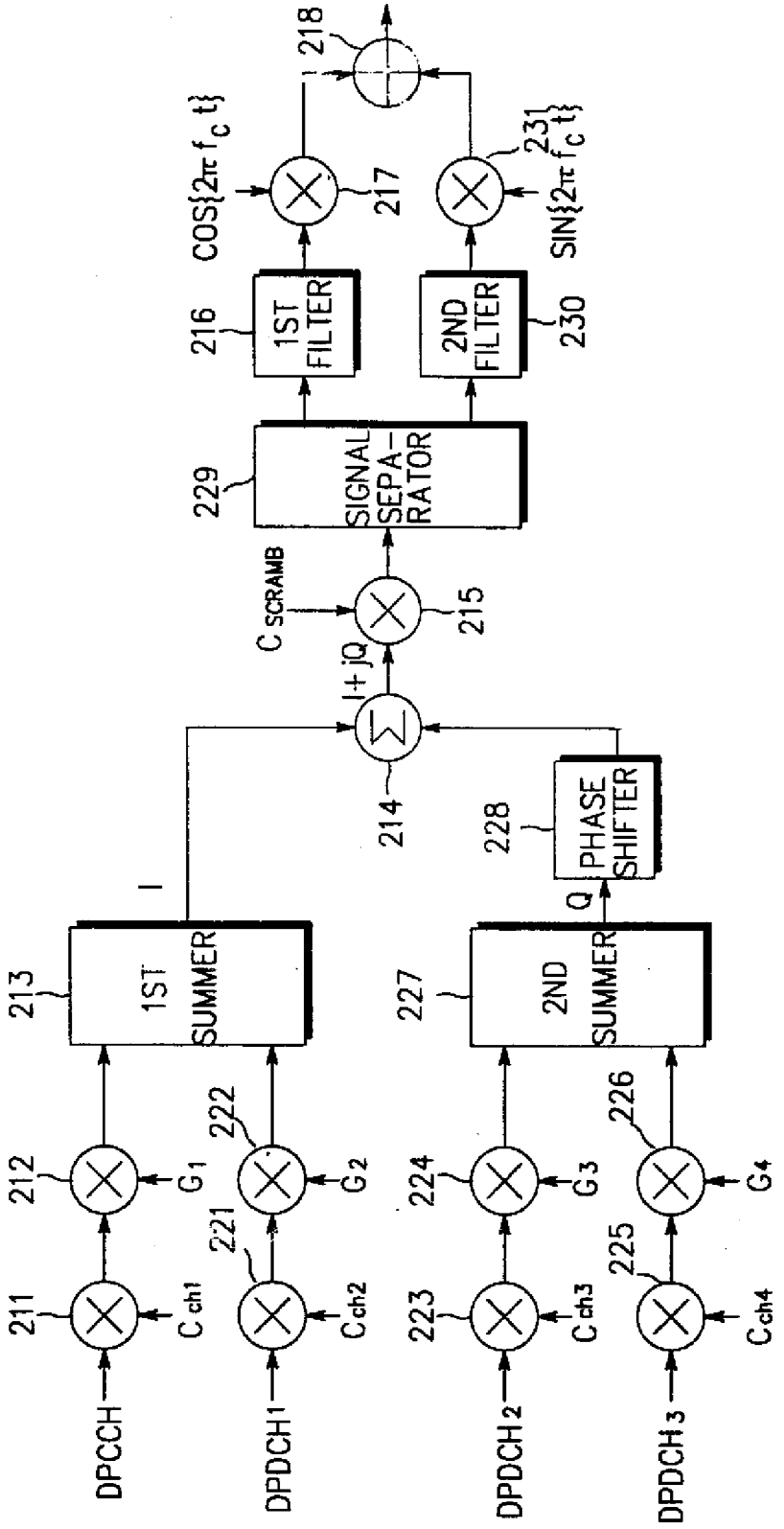

DPCCH
DPDCH1
DPDCH2
DPDCH3
211
212
221
222
223
224
225
226
C ch1
C ch2
C ch3
C ch4
G1
G2
G3
G4
213
1ST SUMMER
227
2ND SUMMER
I
Q
228
PHASE SHIFTER
214
I+jQ
C SCRAMB
215
229
SIGNAL SEPA-RATOR
216
1ST FILTER
230
2ND FILTER
COS{2π fc t}
SIN{2π fc t}
217
231
218

FIG. 3B

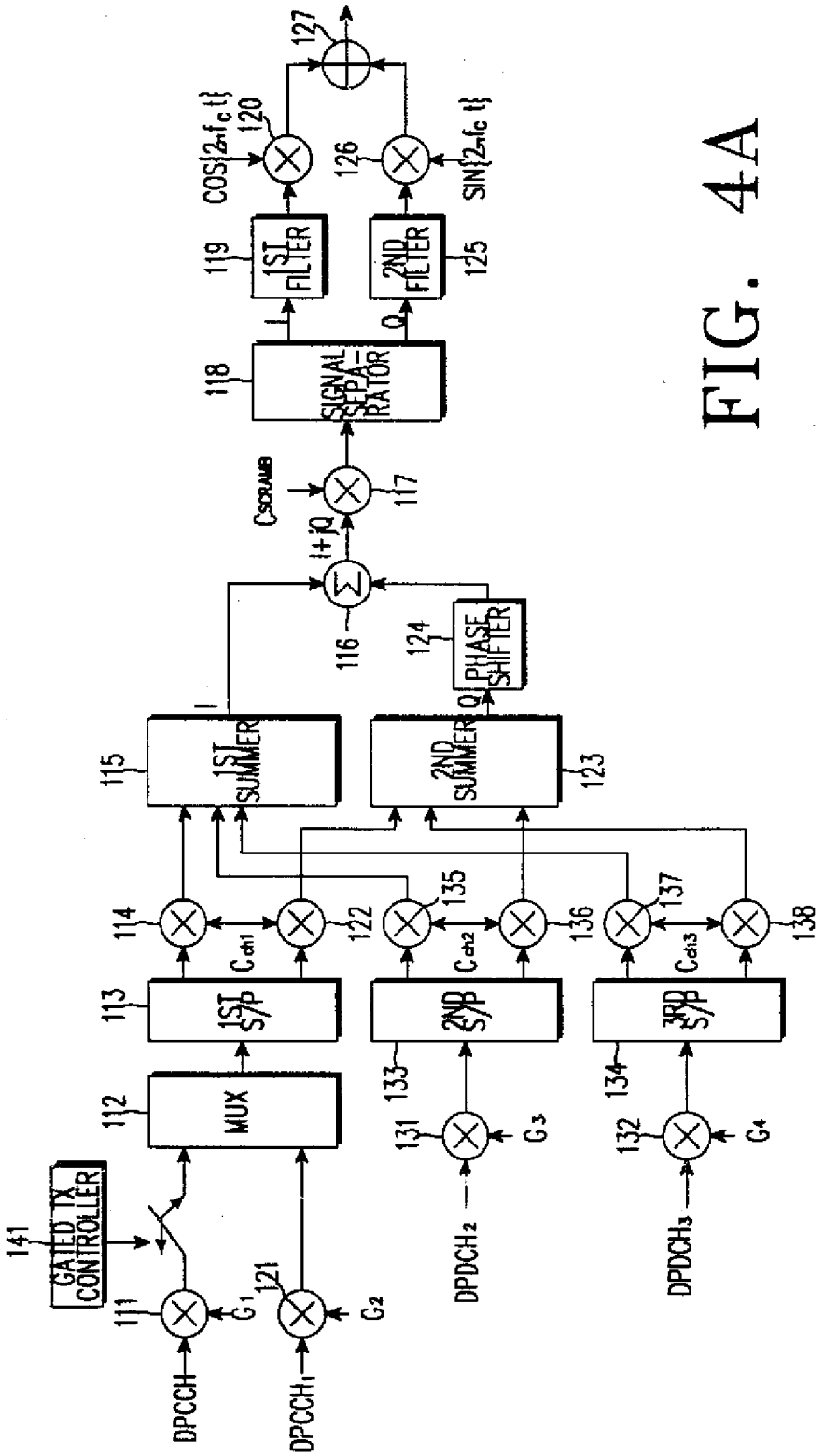

DPCCH
DPCCH1
DPDCH2
DPDCH3
GATED TX CONTROLLER
MUX
1ST S/P
2ND S/P
3RD S/P
1ST SUMMER
2ND SUMMER
PHASE SHIFTER
SIGNAL SEPARATOR
1ST FILTER
2ND FILTER
COS{2πfc t}
SIN{2πfc t}

FIG. 4A

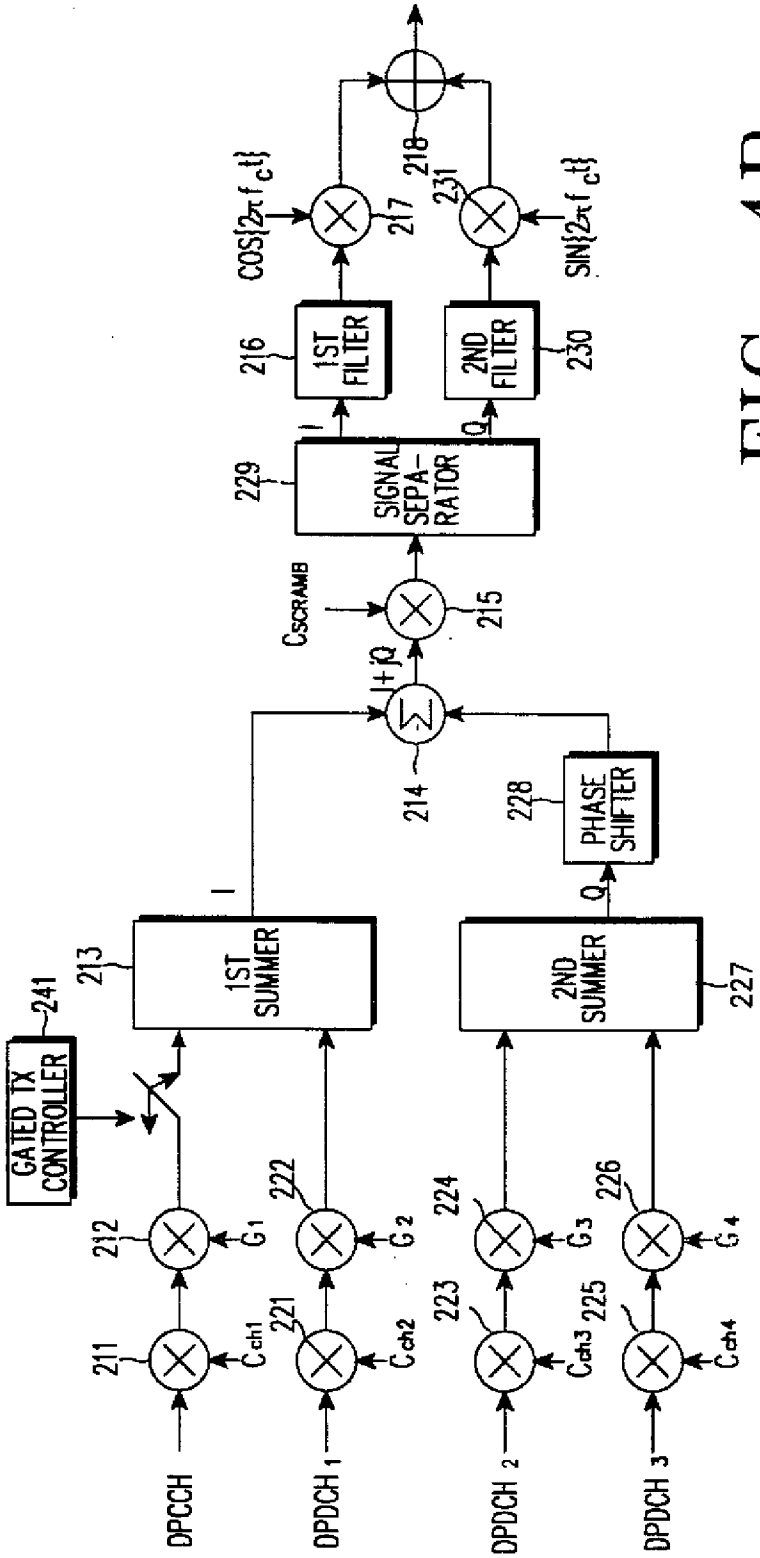

DPCCH
DPDCH 1
DPDCH 2
DPDCH 3
211
212
221
222
223
224
225
226
C_{ch1}
C_{ch2}
C_{ch3}
C_{ch4}
G_1
G_2
G_3
G_4
GATED TX CONTROLLER
241
1ST SUMMER
213
2ND SUMMER
227
I
Q
PHASE SHIFTER
228
214
I+jQ
C_{SCRAMB}
215
SIGNAL SEPA-RATOR
229
1ST FILTER
216
2ND FILTER
230
$\cos\{2\pi f_c t\}$
$\sin\{2\pi f_c t\}$
217
231
218

FIG. 4B

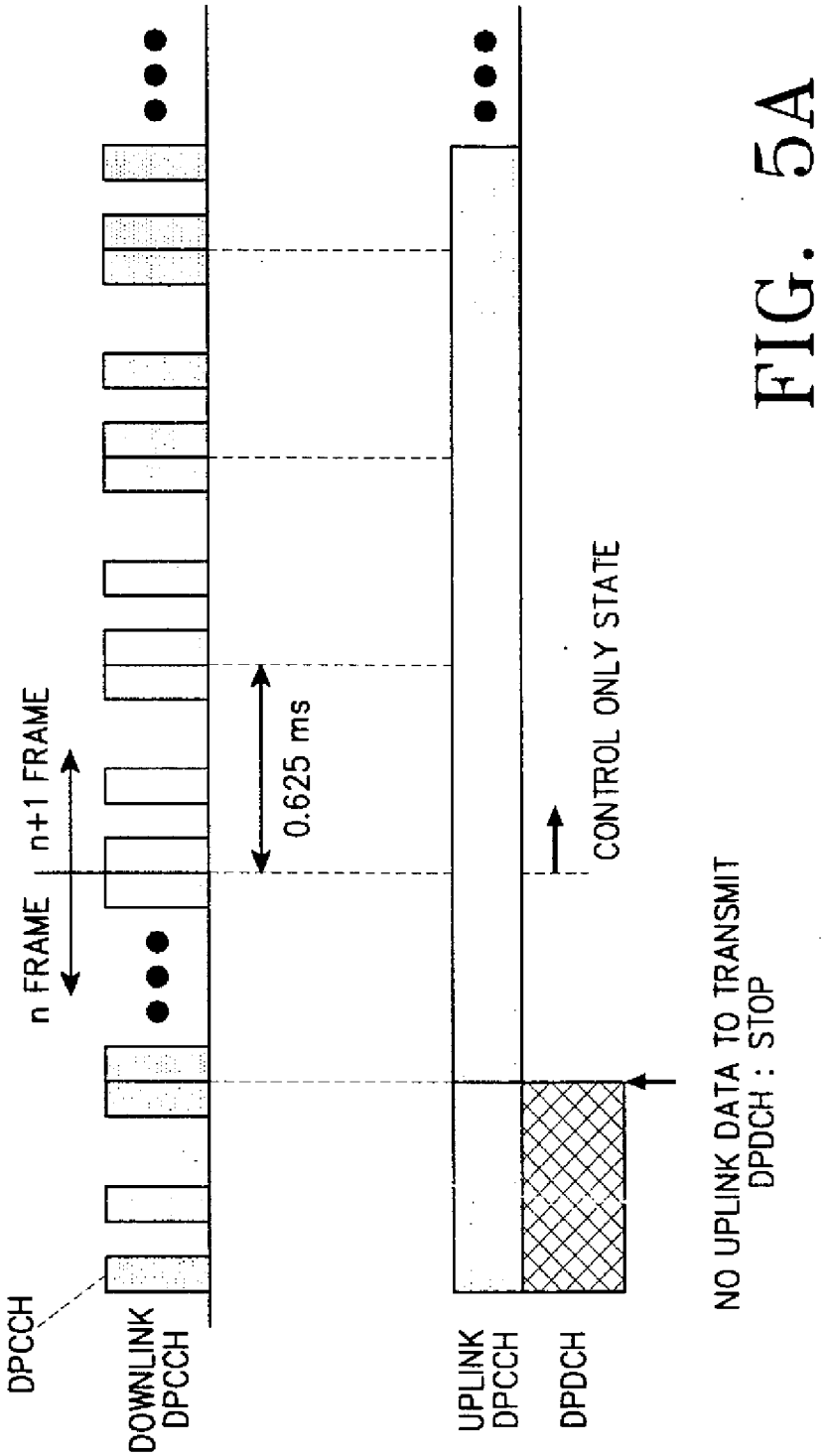

DPCCH
DOWNLINK DPCCH
n FRAME
n+1 FRAME
0.625 ms
UPLINK DPCCH
DPDCH
CONTROL ONLY STATE
NO UPLINK DATA TO TRANSMIT
DPDCH : STOP

FIG. 5A

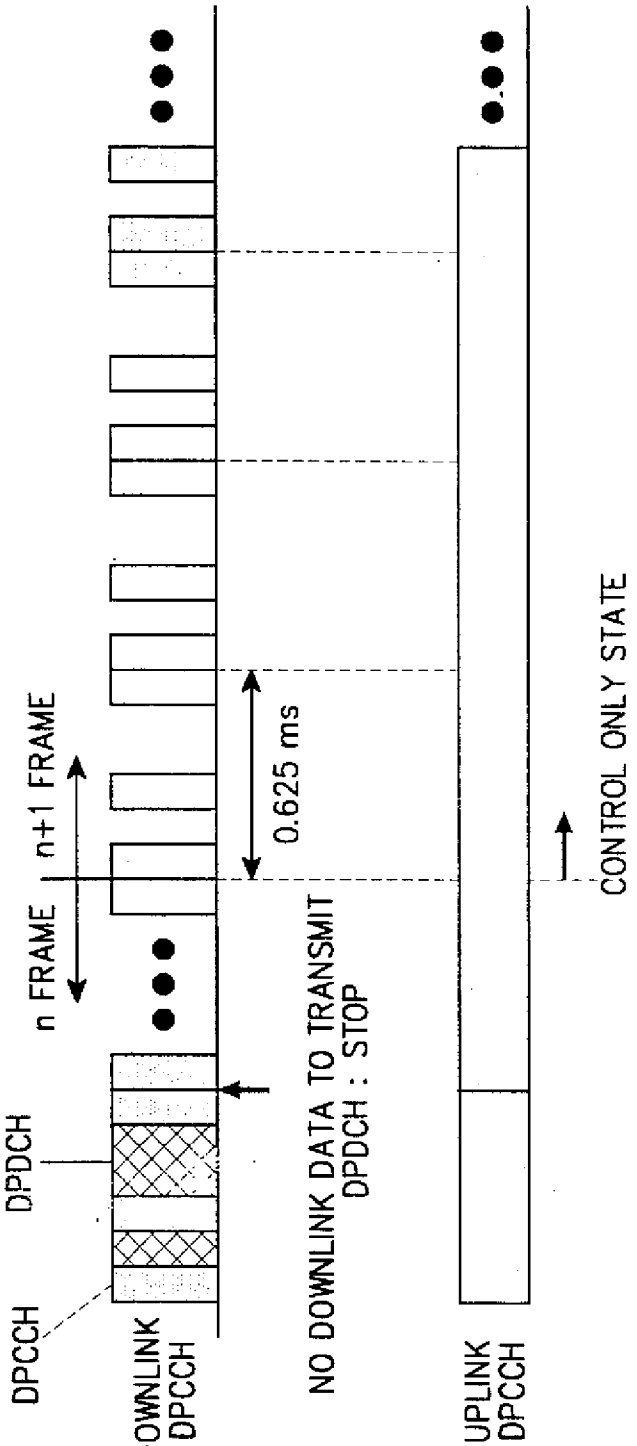

DPCCH
DPDCH
n FRAME
n+1 FRAME
DOWNLINK DPCCH
NO DOWNLINK DATA TO TRANSMIT
DPDCH : STOP
0.625 ms
UPLINK DPCCH
CONTROL ONLY STATE

FIG. 5B

FIG. 6A

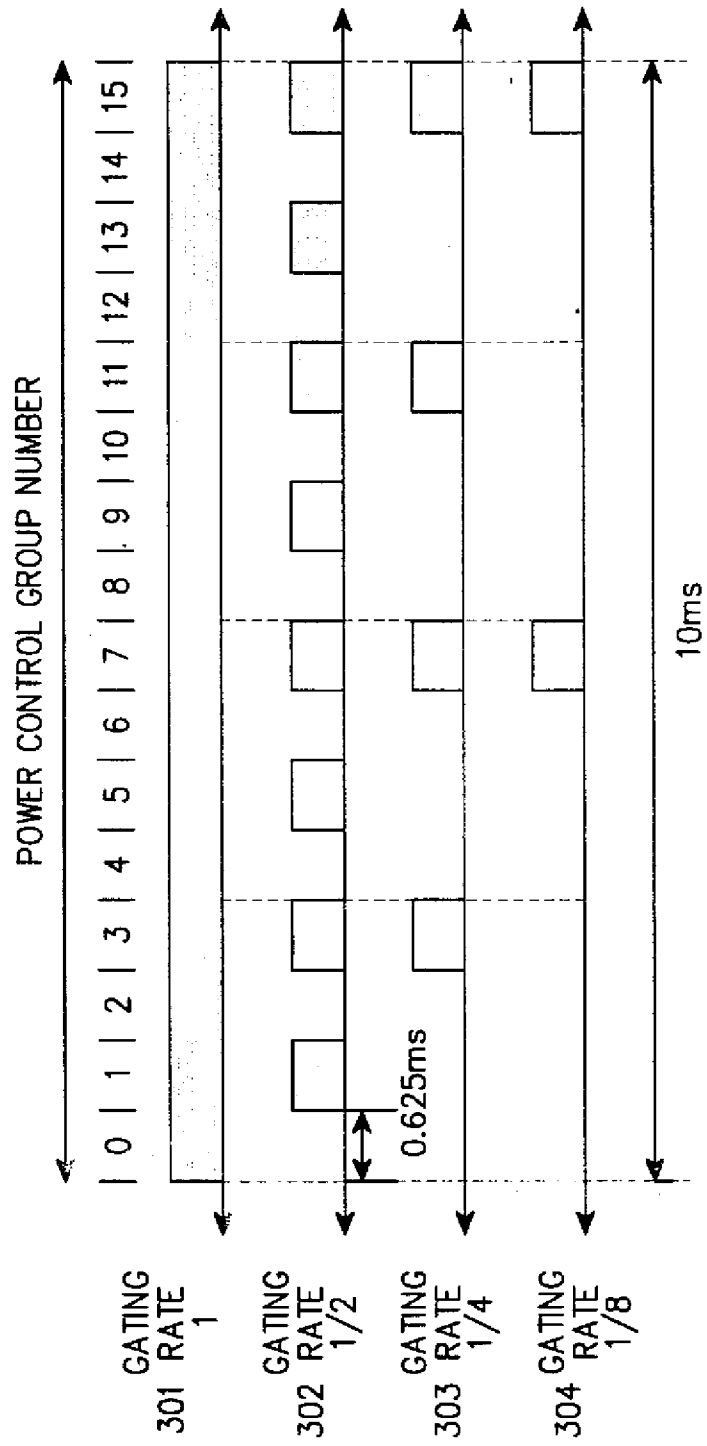

POWER CONTROL GROUP NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0.625ms
10ms
GATING RATE 1
301
GATING RATE 1/2
302
GATING RATE 1/4
303
GATING RATE 1/8
304

FIG. 6B

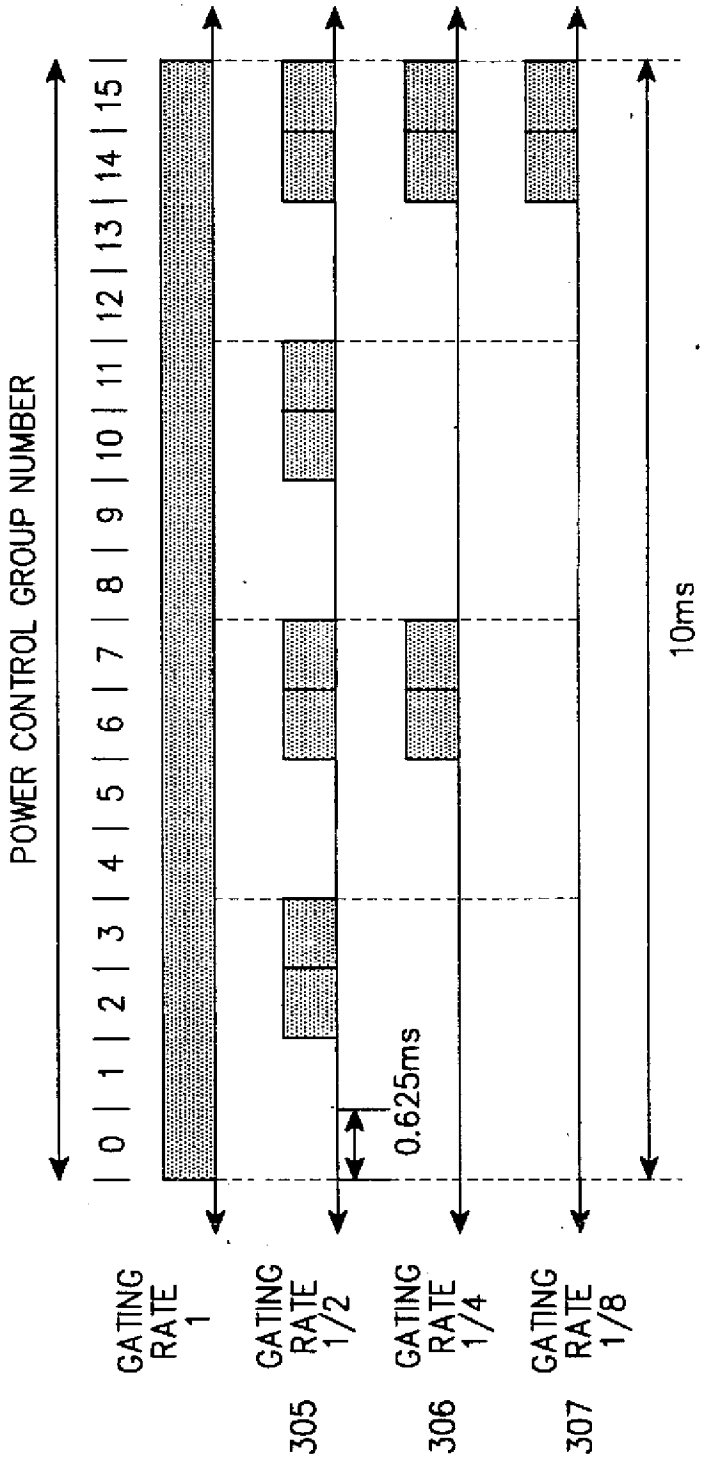

POWER CONTROL GROUP NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0.625ms
10ms
GATING RATE 1
GATING RATE 1/2
GATING RATE 1/4
GATING RATE 1/8
305
306
307

FIG. 7A

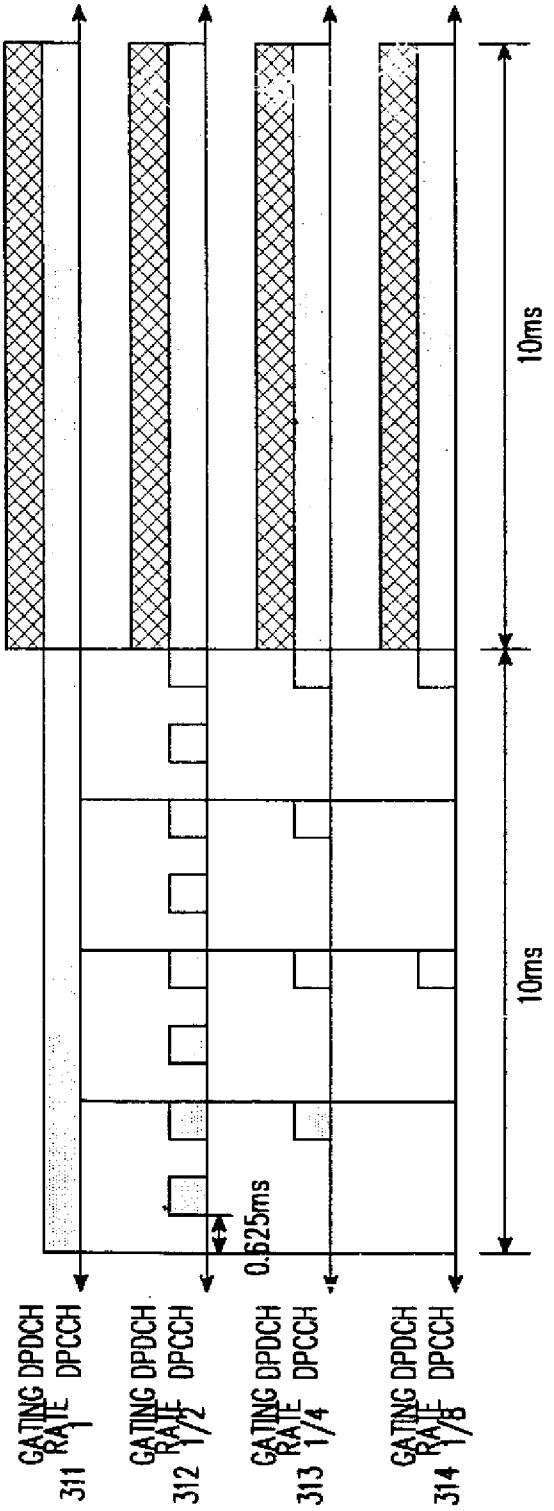

GATING RATE 1
DPDCH
DPCCH
311
GATING RATE 1/2
DPDCH
DPCCH
312
GATING RATE 1/4
DPDCH
DPCCH
313
GATING RATE 1/8
DPDCH
DPCCH
314
0.625ms
10ms
10ms

FIG. 7B

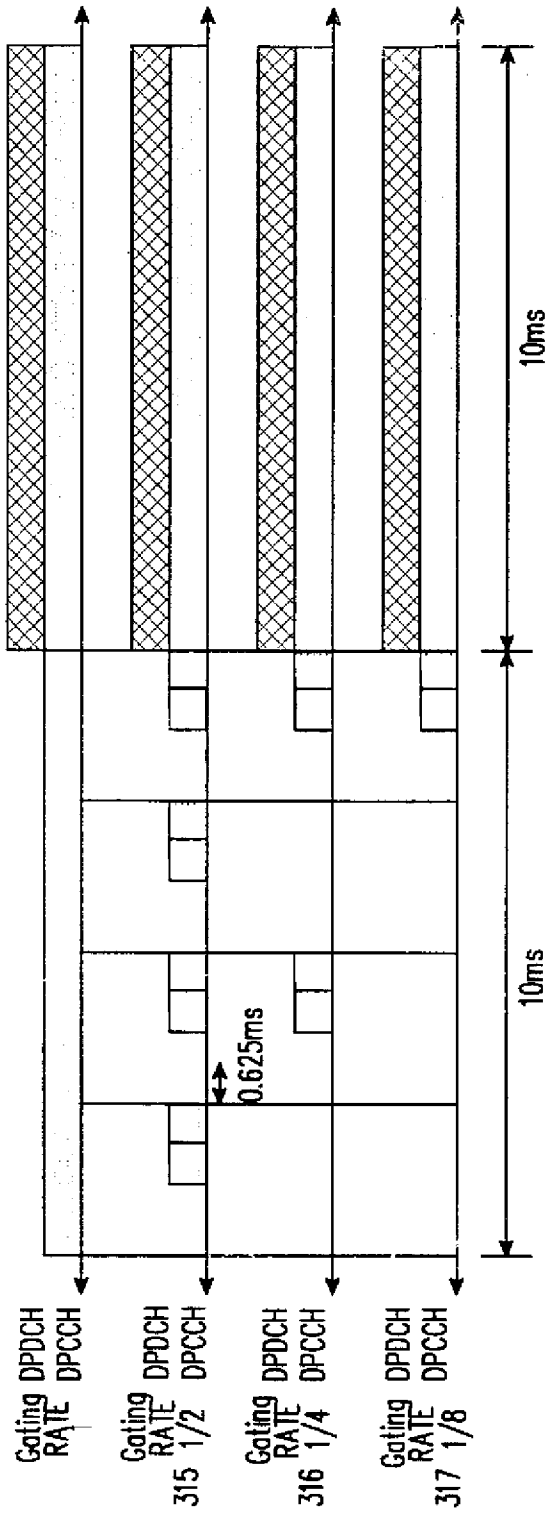

Gating RATE DPDCH DPCCH
Gating RATE 1/2 315 DPDCH DPCCH
Gating RATE 1/4 316 DPDCH DPCCH
Gating RATE 1/8 317 DPDCH DPCCH
0.625ms
10ms
10ms

FIG. 8A

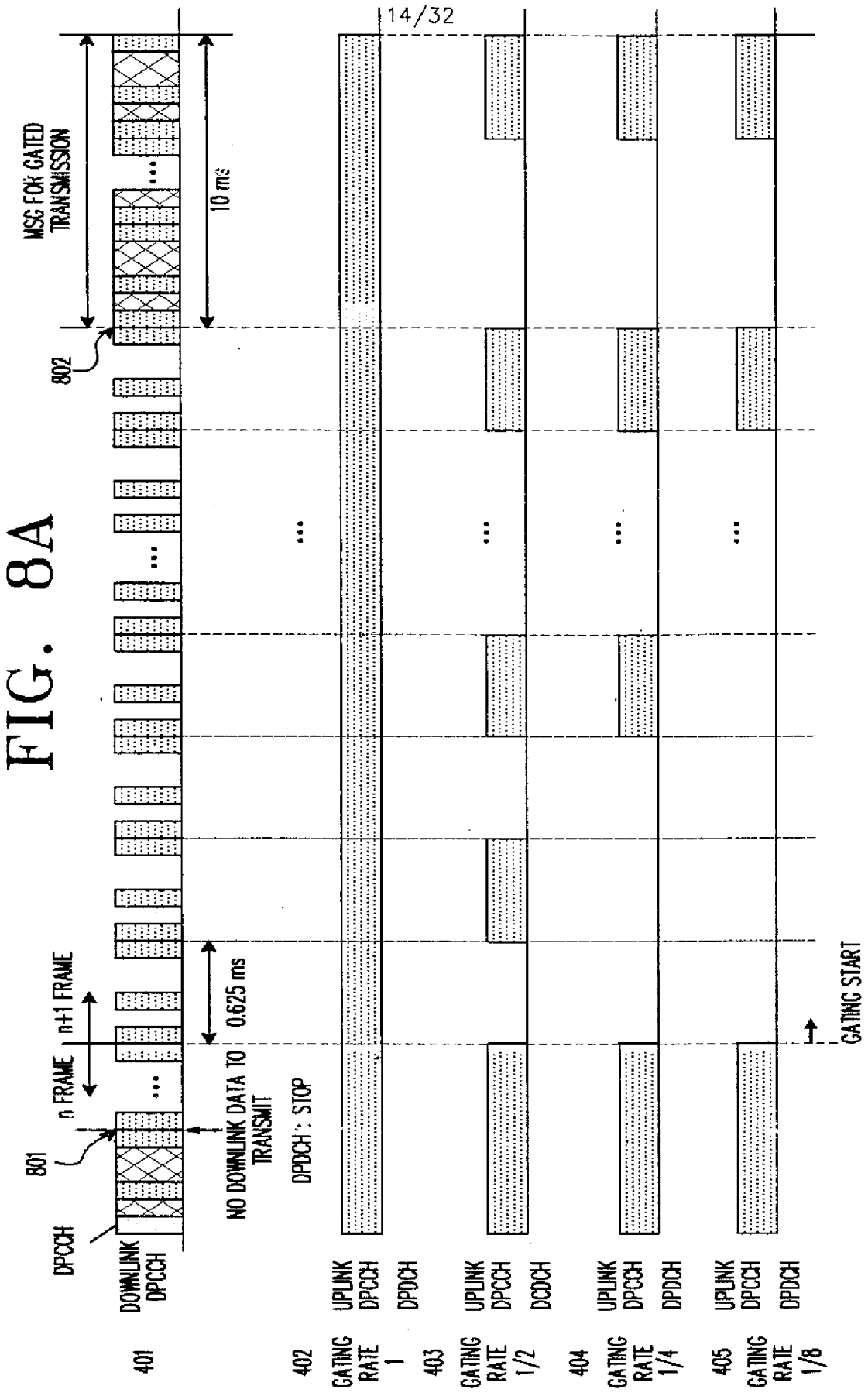
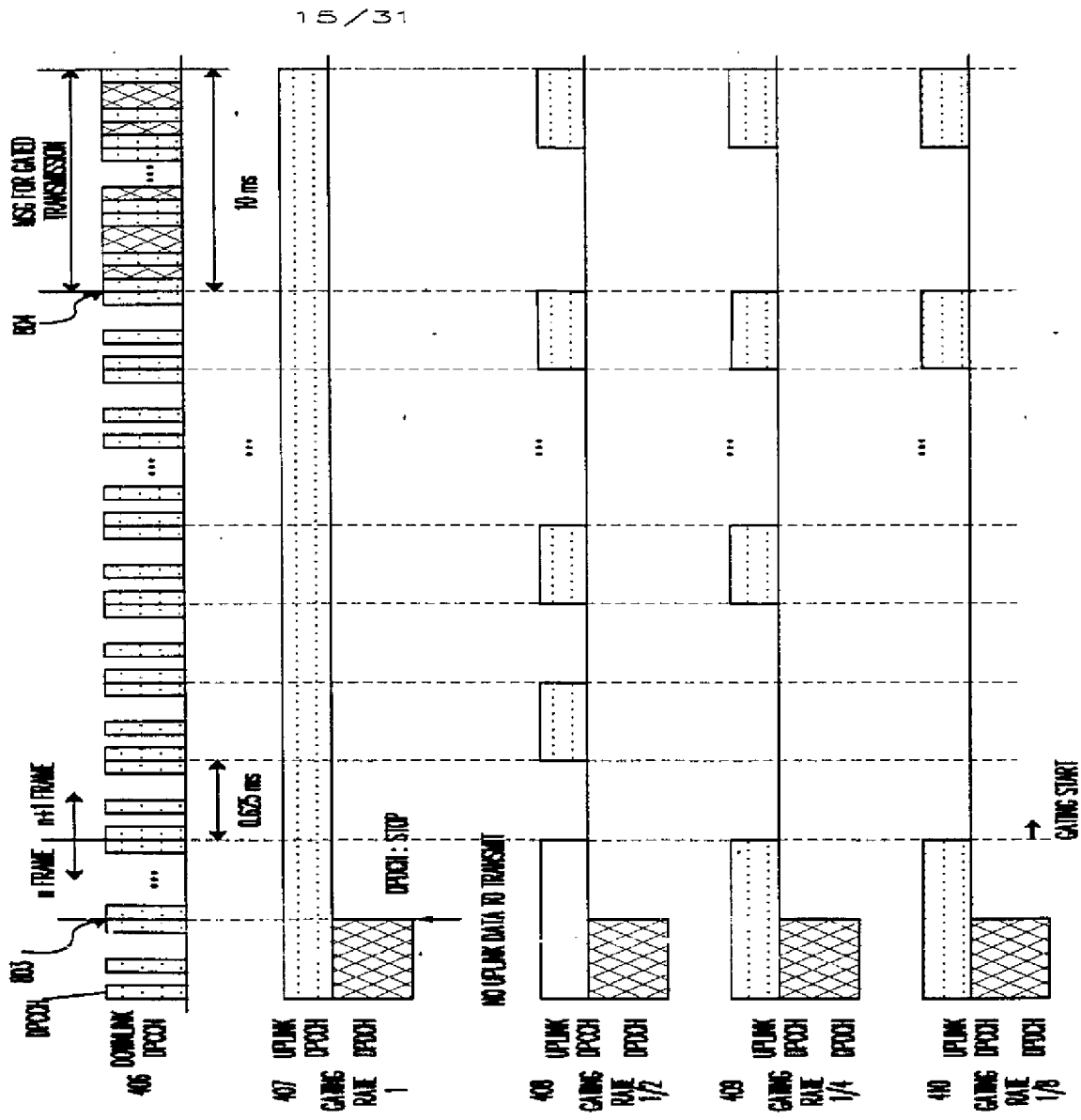

MSG FOR GATED TRANSMISSION
802
10 ms
801
n FRAME
n+1 FRAME
0.625 ms
NO DOWNLINK DATA TO TRANSMIT
DPCCH
DOWNLINK DPCCH
DPDCH : STOP
GATING START
401
402
GATING RATE 1
UPLINK DPCCH
DPDCH
403
GATING RATE 1/2
UPLINK DPCCH
DPDCH
404
GATING RATE 1/4
UPLINK DPCCH
DPDCH
405
GATING RATE 1/8
UPLINK DPCCH
DPDCH

FIG. 8B


15/31
MSG FOR GATED TRANSMISSION
BCH
10 ms
n FRAME
n+1 FRAME
0.625 ms
403
DPCCH
406 DOWNLINK DPCCH
407 UPLINK DPCCH GATING RATE 1
EPCCH : STOP
NO UPLINK DATA TO TRANSMIT
408 UPLINK DPCCH GATING RATE 1/2
409 UPLINK DPCCH GATING RATE 1/4
410 UPLINK DPCCH GATING RATE 1/8
GATING START

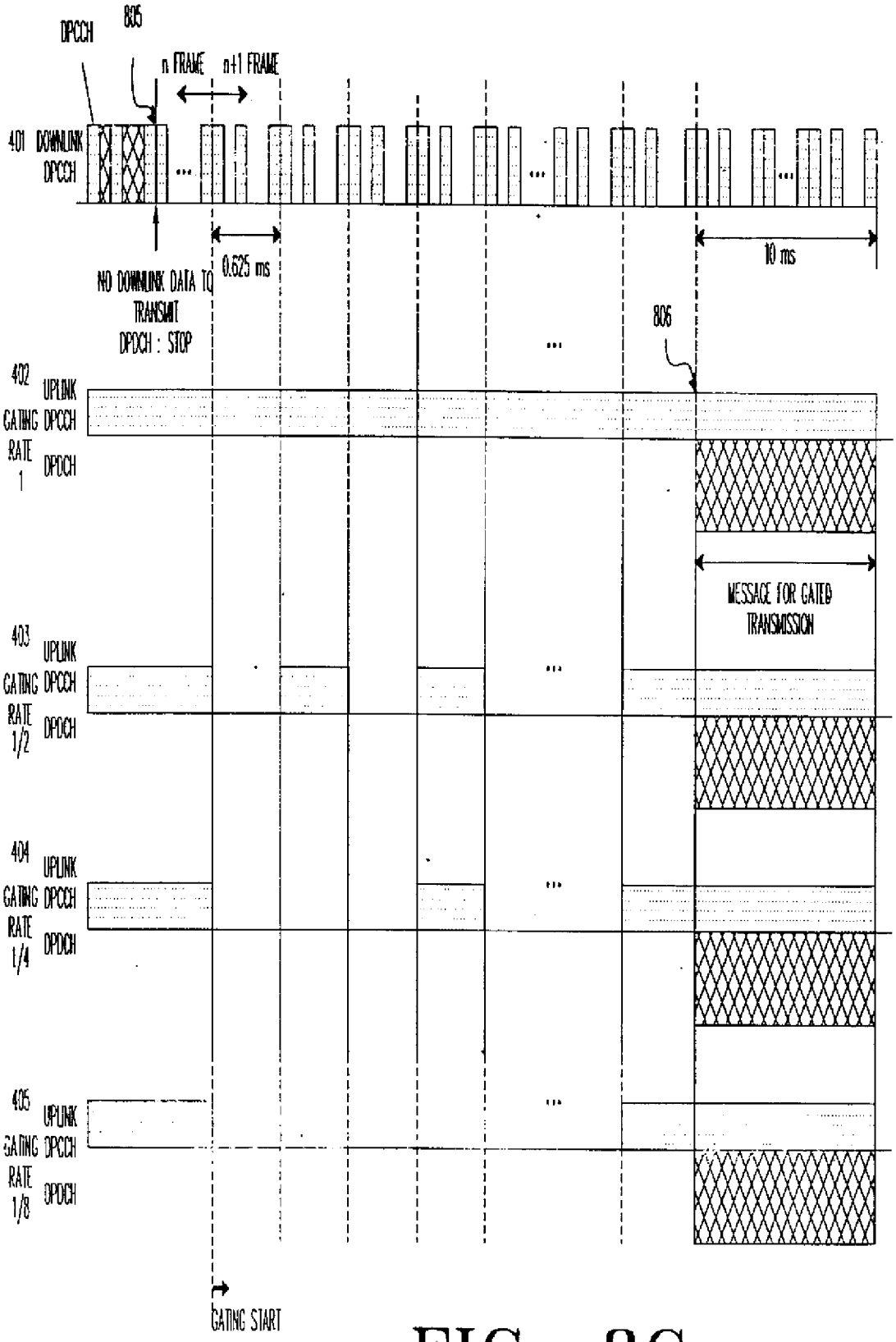

DPCCH
805
n FRAME
n+1 FRAME
401 DOWNLINK DPCCH
0.625 ms
10 ms
NO DOWNLINK DATA TO TRANSMIT DPCCH : STOP
806
402 UPLINK DPCCH GATING RATE 1 DPDCH
MESSAGE FOR GATED TRANSMISSION
403 UPLINK DPCCH GATING RATE 1/2 DPDCH
404 UPLINK DPCCH GATING RATE 1/4 DPDCH
405 UPLINK DPCCH GATING RATE 1/8 DPDCH
GATING START

FIG. 8C

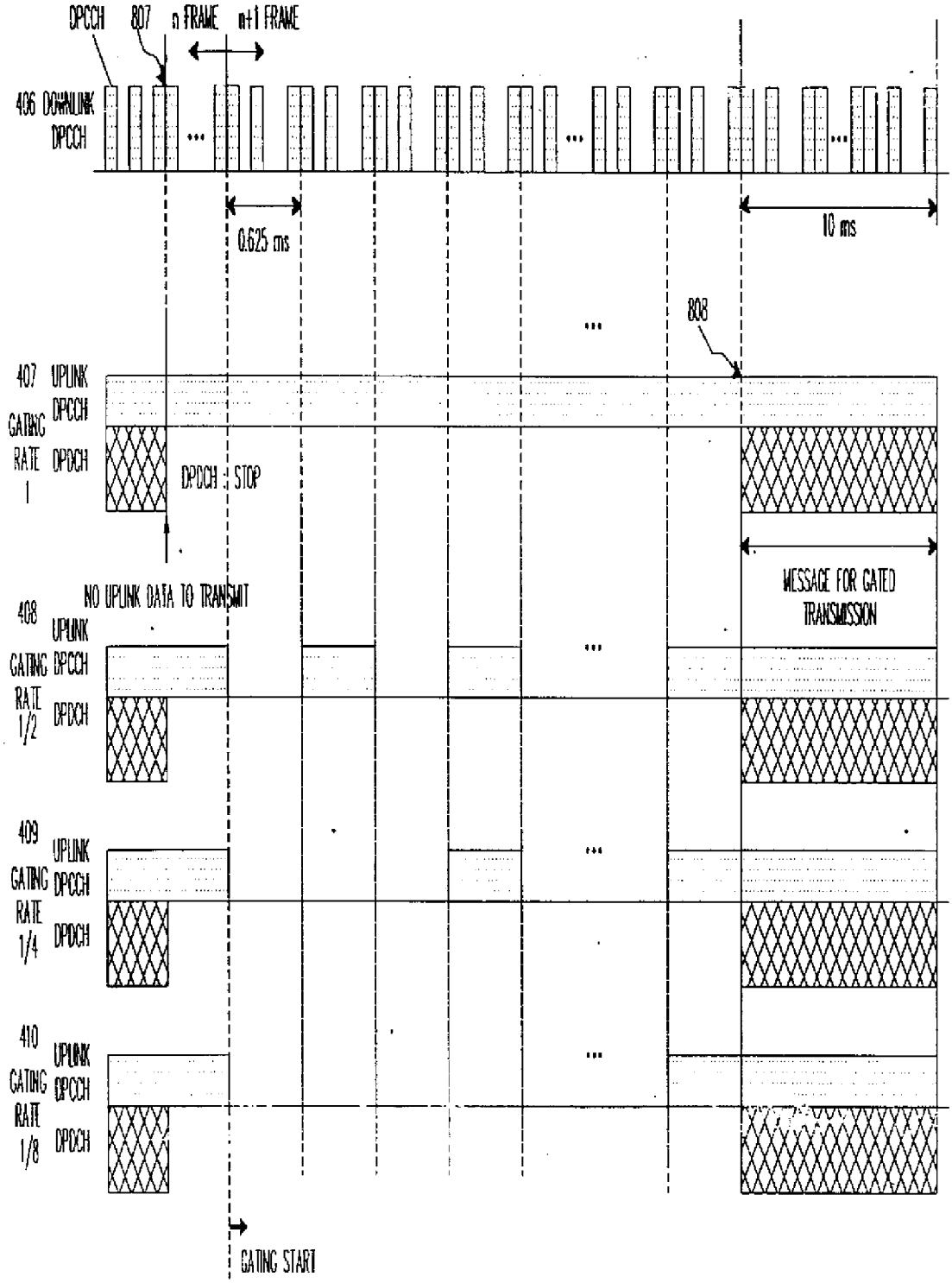

DPCCH
807
n FRAME
n+1 FRAME
406 DOWNLINK DPCCH
0.625 ms
10 ms
808
407 UPLINK DPCCH
GATING RATE 1
DPDCH
DPCCH : STOP
NO UPLINK DATA TO TRANSMIT
MESSAGE FOR GATED TRANSMISSION
408 UPLINK DPCCH
GATING RATE 1/2
DPDCH
409 UPLINK DPCCH
GATING RATE 1/4
DPDCH
410 UPLINK DPCCH
GATING RATE 1/8
DPDCH
GATING START

FIG. 8D

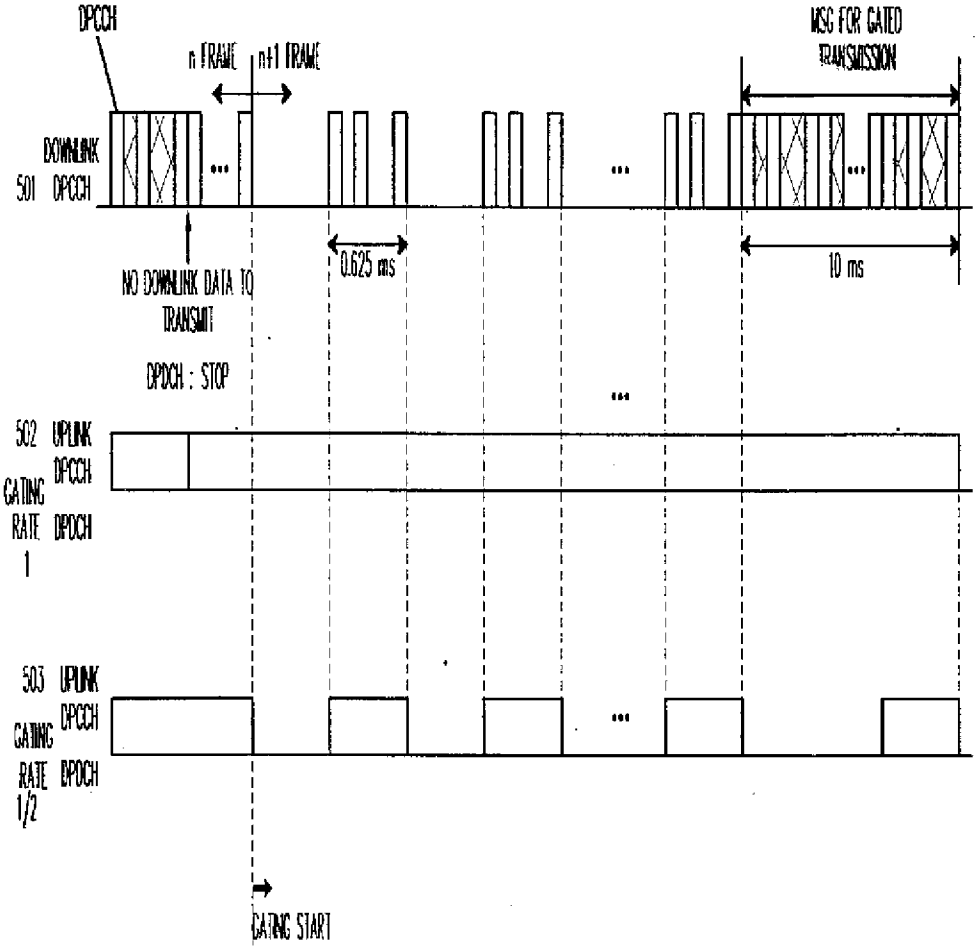

DPCCH
n FRAME
n+1 FRAME
MSG FOR GATED TRANSMISSION
DOWNLINK
501 DPCCH
0.625 ms
10 ms
NO DOWNLINK DATA TO TRANSMIT
DPDCH : STOP
502 UPLINK DPCCH
GATING RATE 1
DPDCH
503 UPLINK DPCCH
GATING RATE 1/2
DPDCH
GATING START

FIG. 9A

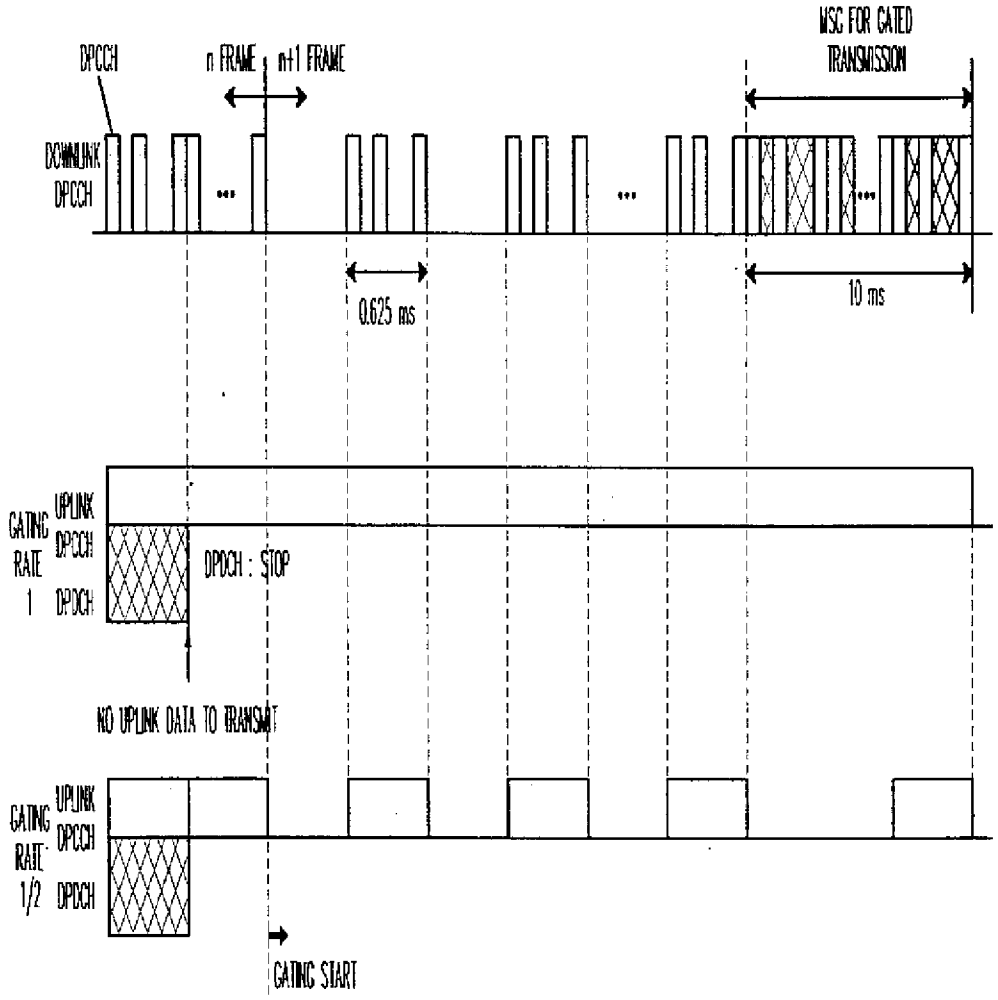

DPCCH
n FRAME
n+1 FRAME
WSC FOR GATED TRANSMISSION
DOWNLINK DPCCH
0.625 ms
10 ms
GATING RATE 1
UPLINK DPCCH
DPDCH
DPDCH : STOP
NO UPLINK DATA TO TRANSMIT
GATING RATE 1/2
UPLINK DPCCH
DPDCH
GATING START

FIG. 9B

FIG. 10A

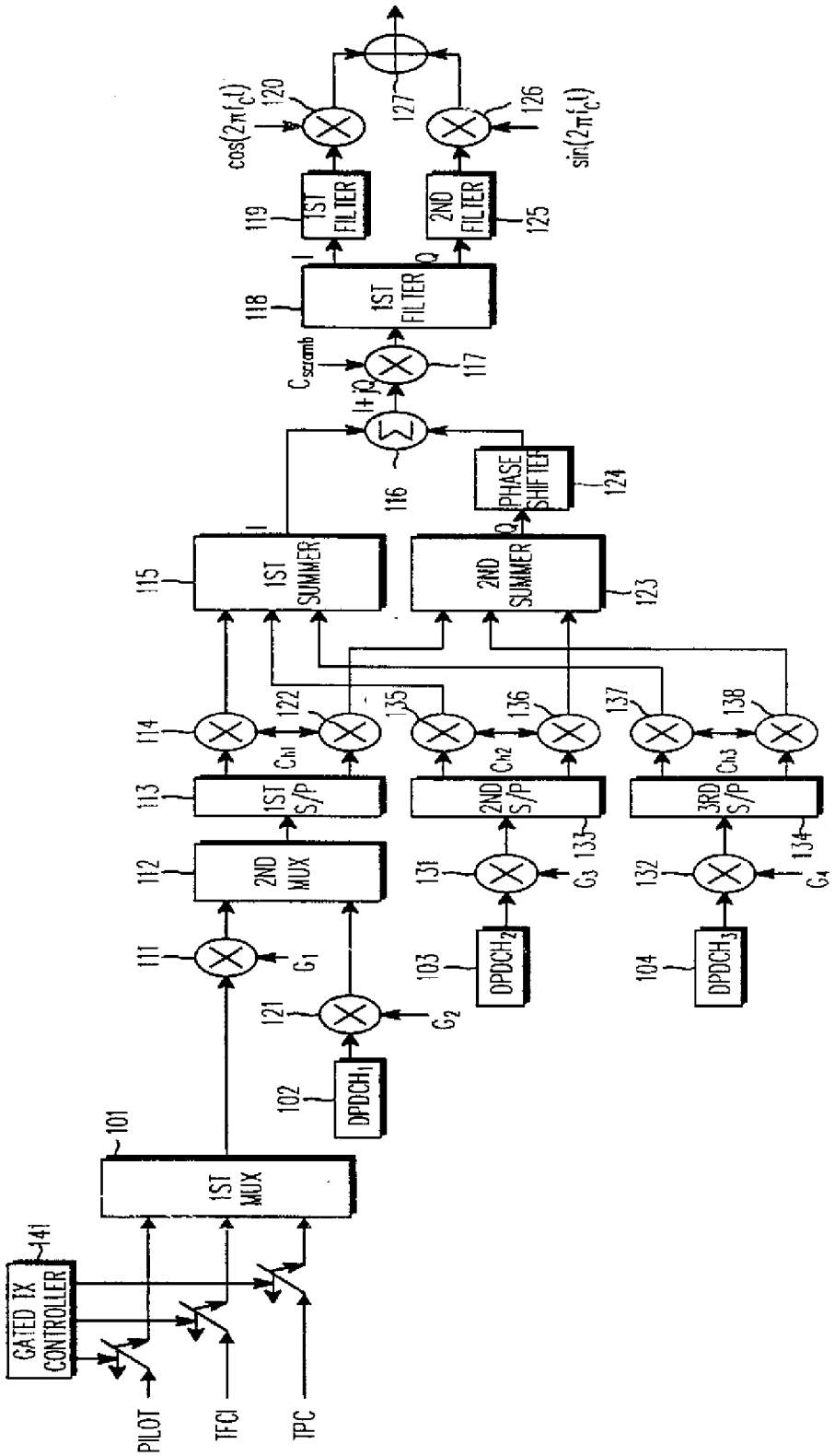
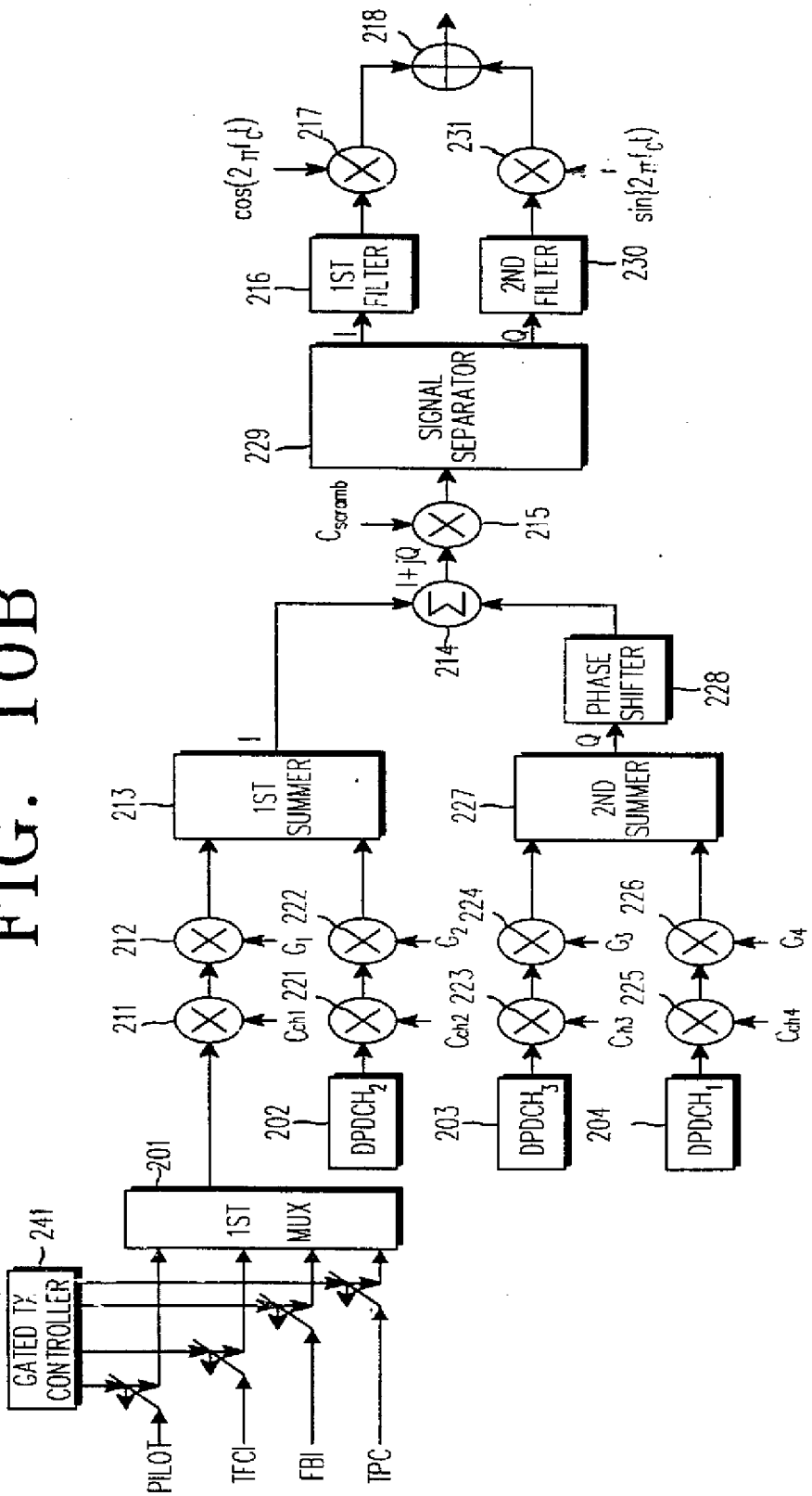

GATED TX CONTROLLER
141
PILOT
TFCI
TPC
1ST MUX
101
DPDCH1
102
DPDCH2
103
DPDCH3
104
2ND MUX
112
1ST S/P
113
2ND S/P
3RD S/P
1ST SUMMER
115
2ND SUMMER
123
PHASE SHIFTER
124
1ST FILTER
118
2ND FILTER
125
cos(2πfct)
sin(2πfct)
120
126
127
116
117
119
111
121
131
132
133
134
135
136
137
138
122

FIG. 10B


GATED TX CONTROLLER
241
PILOT
TFCI
FBI
TPC
1ST MUX
201
DPDCH2
202
DPDCH3
203
DPDCH1
204
Ch1 221
Ch2 223
Ch3 225
Ch4
G1 222
G2 224
G3 226
G4
211
212
1ST SUMMER
213
2ND SUMMER
227
PHASE SHIFTER
228
I+jQ
214
Cscramb
215
SIGNAL SEPARATOR
229
1ST FILTER
216
2ND FILTER
230
cos(2πfct)
217
sin(2πfct)
231
218

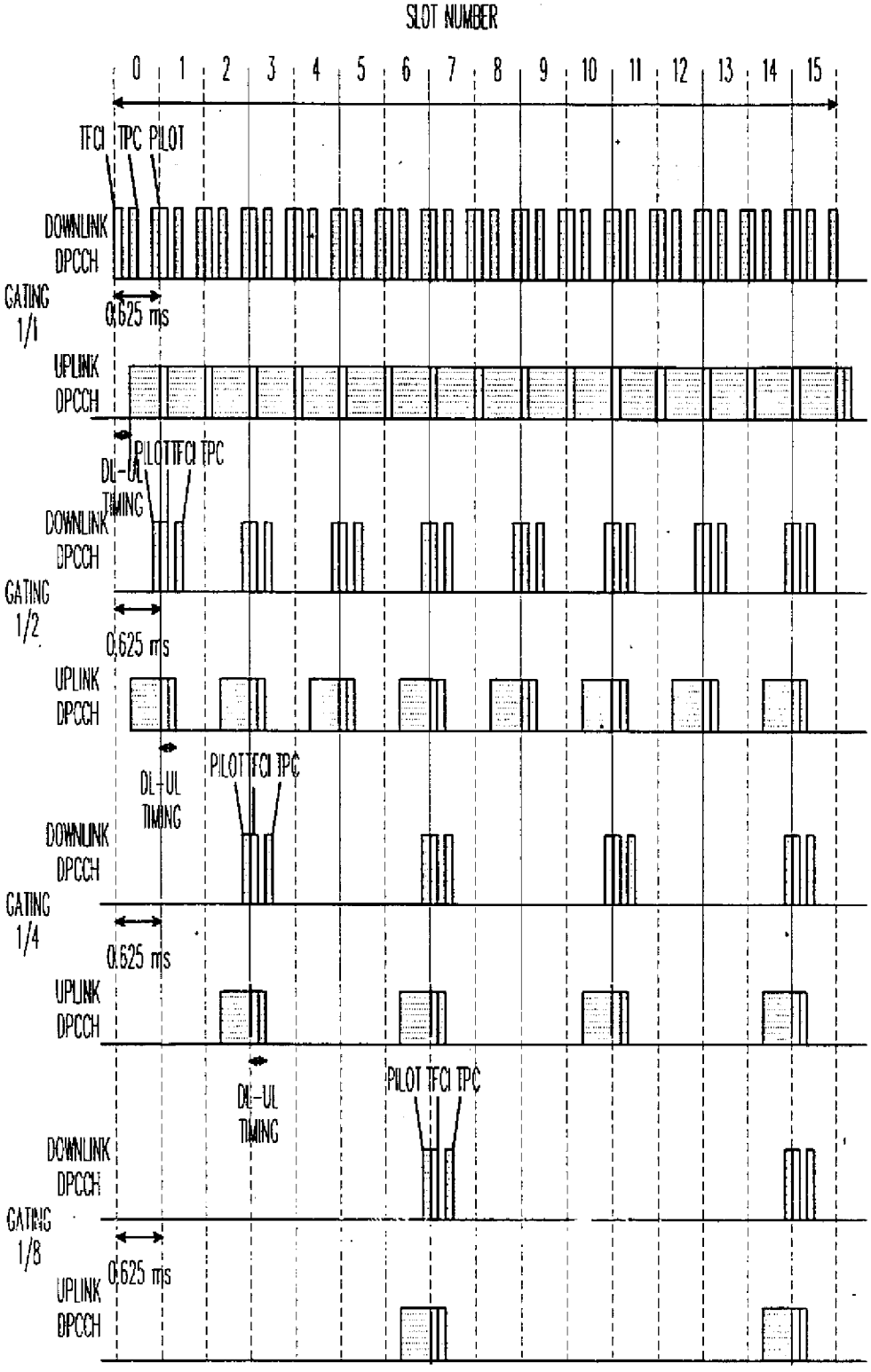

SLOT NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
TFCI TPC PILOT
DOWNLINK DPCCH
GATING 1/1
0.625 ms
UPLINK DPCCH
PILOT TFCI TPC
DL-UL TIMING
DOWNLINK DPCCH
GATING 1/2
0.625 ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING 1/4
0.625 ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING 1/8
0.625 ms
UPLINK DPCCH

FIG. 11A

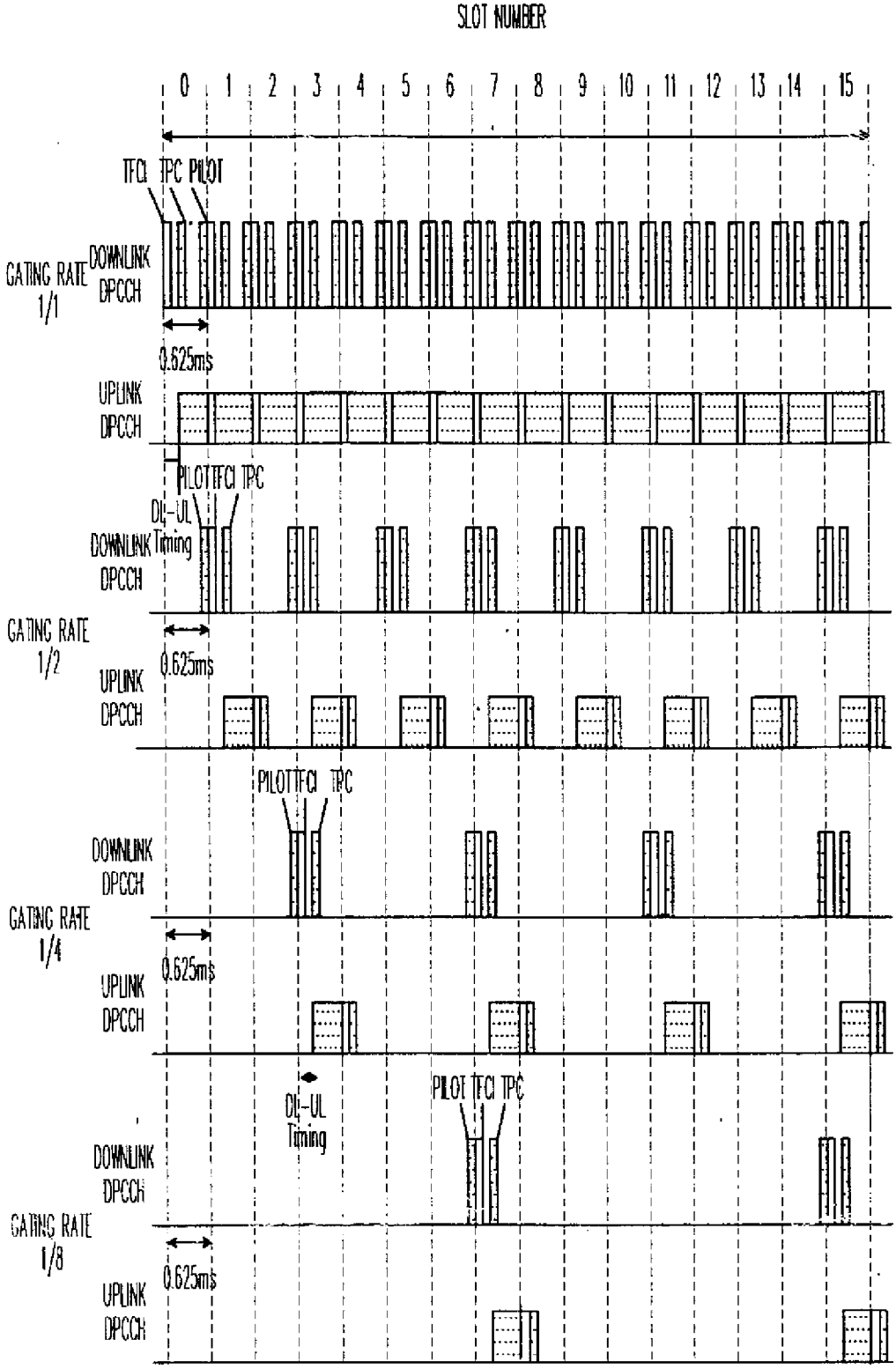

SLOT NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
TFCI TPC PILOT
GATING RATE 1/1
DOWNLINK DPCCH
0.625ms
UPLINK DPCCH
PILOT TFCI TPC
DL-UL Timing
DOWNLINK DPCCH
GATING RATE 1/2
0.625ms
UPLINK DPCCH
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/4
0.625ms
UPLINK DPCCH
DL-UL Timing
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/8
0.625ms
UPLINK DPCCH

FIG. 11B

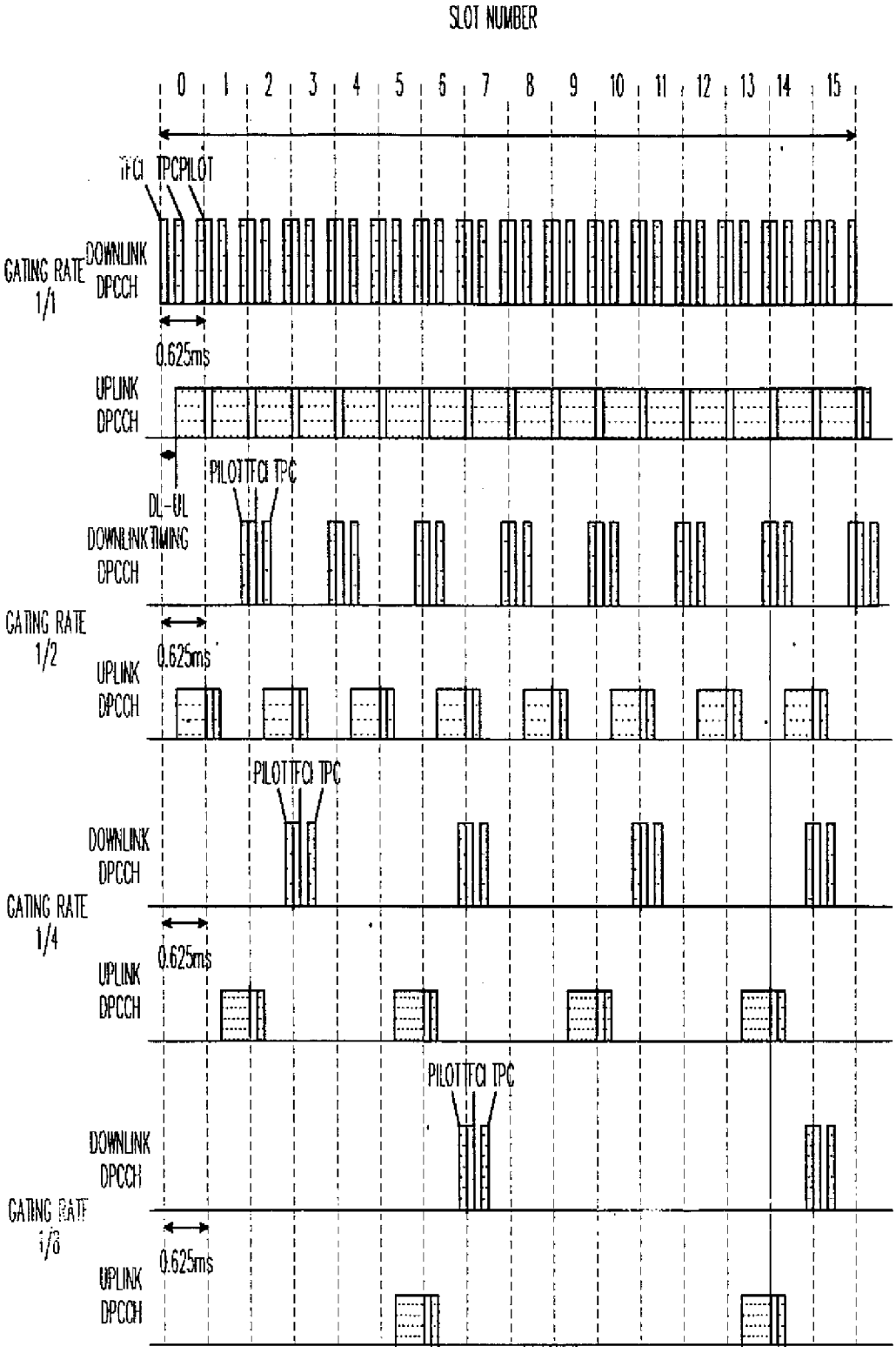

SLOT NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
TFCI TPC PILOT
GATING RATE 1/1
DOWNLINK DPCCH
0.625ms
UPLINK DPCCH
PILOT TFCI TPC
DL-UL TIMING
DOWNLINK DPCCH
GATING RATE 1/2
0.625ms
UPLINK DPCCH
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/4
0.625ms
UPLINK DPCCH
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/8
0.625ms
UPLINK DPCCH

FIG. 11C

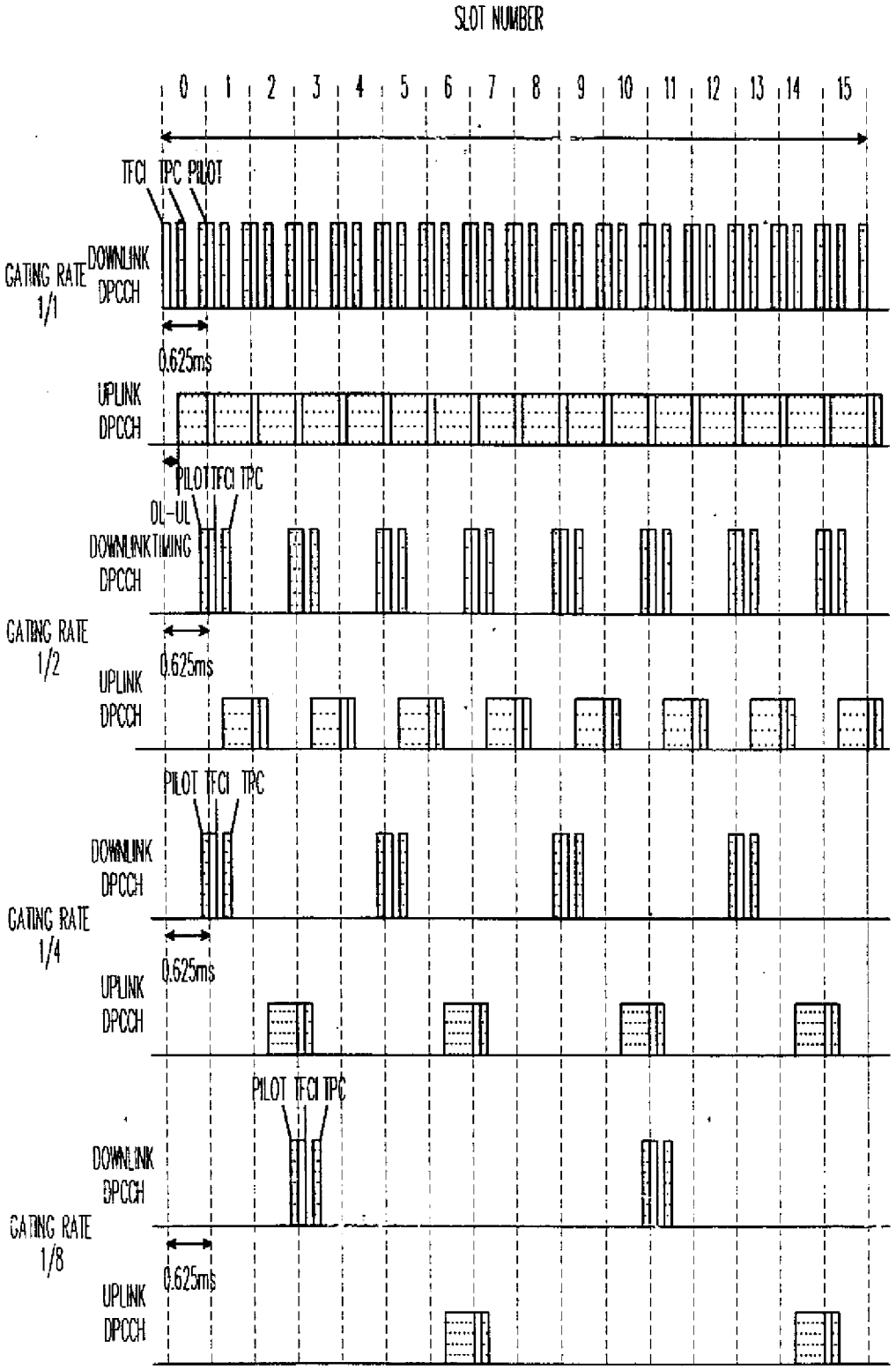

SLOT NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
TFCI TPC PILOT
GATING RATE 1/1
DOWNLINK DPCCH
0.625ms
UPLINK DPCCH
PILOT TFCI TPC
OL-UL TIMING
DOWNLINK DPCCH
GATING RATE 1/2
0.625ms
UPLINK DPCCH
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/4
0.625ms
UPLINK DPCCH
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/8
0.625ms
UPLINK DPCCH

FIG. 11D

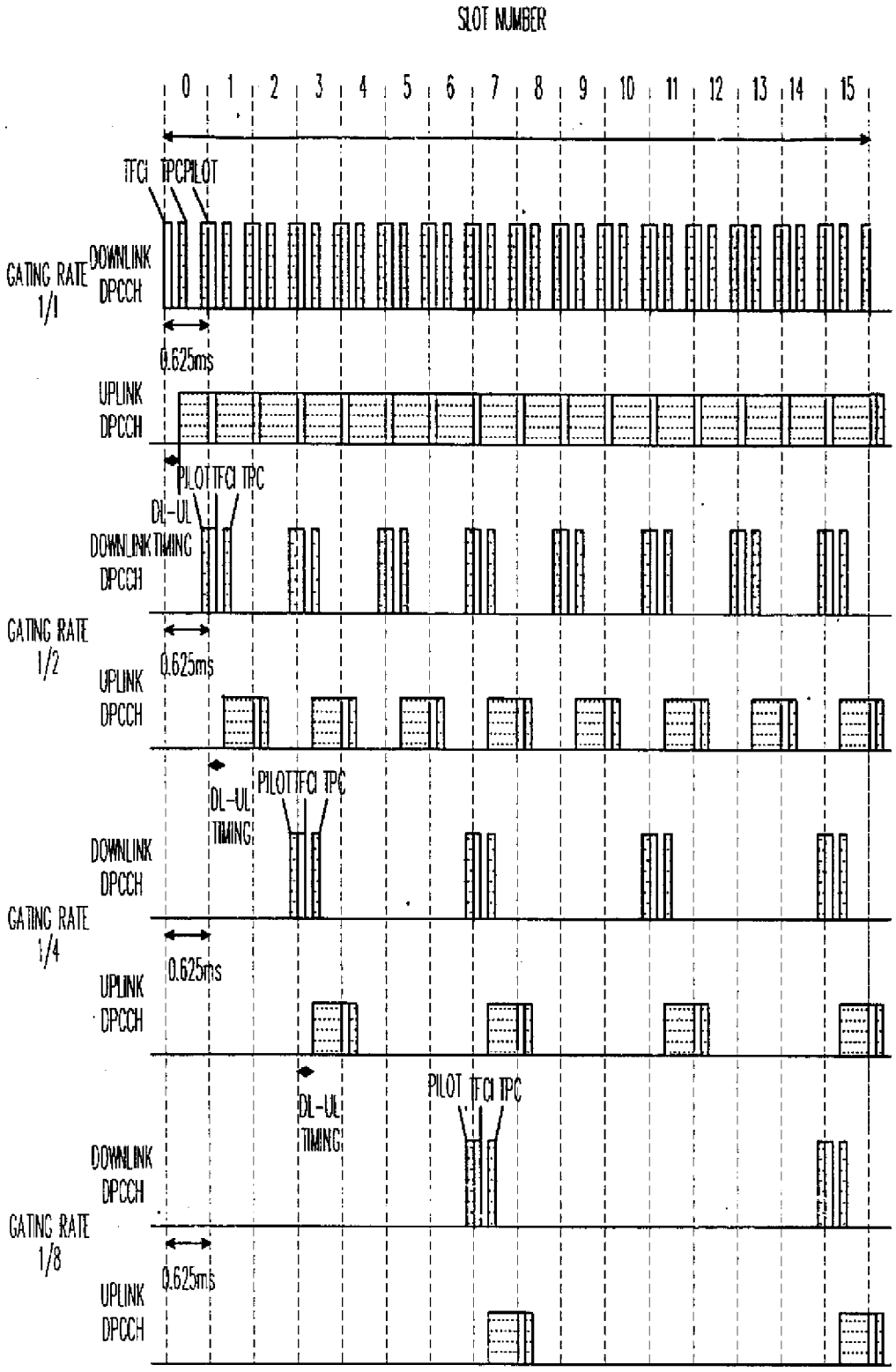

SLOT NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
TFCI TPC PILOT
GATING RATE 1/1
DOWNLINK DPCCH
0.625ms
UPLINK DPCCH
PILOT TFCI TPC
DL-UL TIMING
DOWNLINK DPCCH
GATING RATE 1/2
0.625ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/4
0.625ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/8
0.625ms
UPLINK DPCCH

FIG. 11E

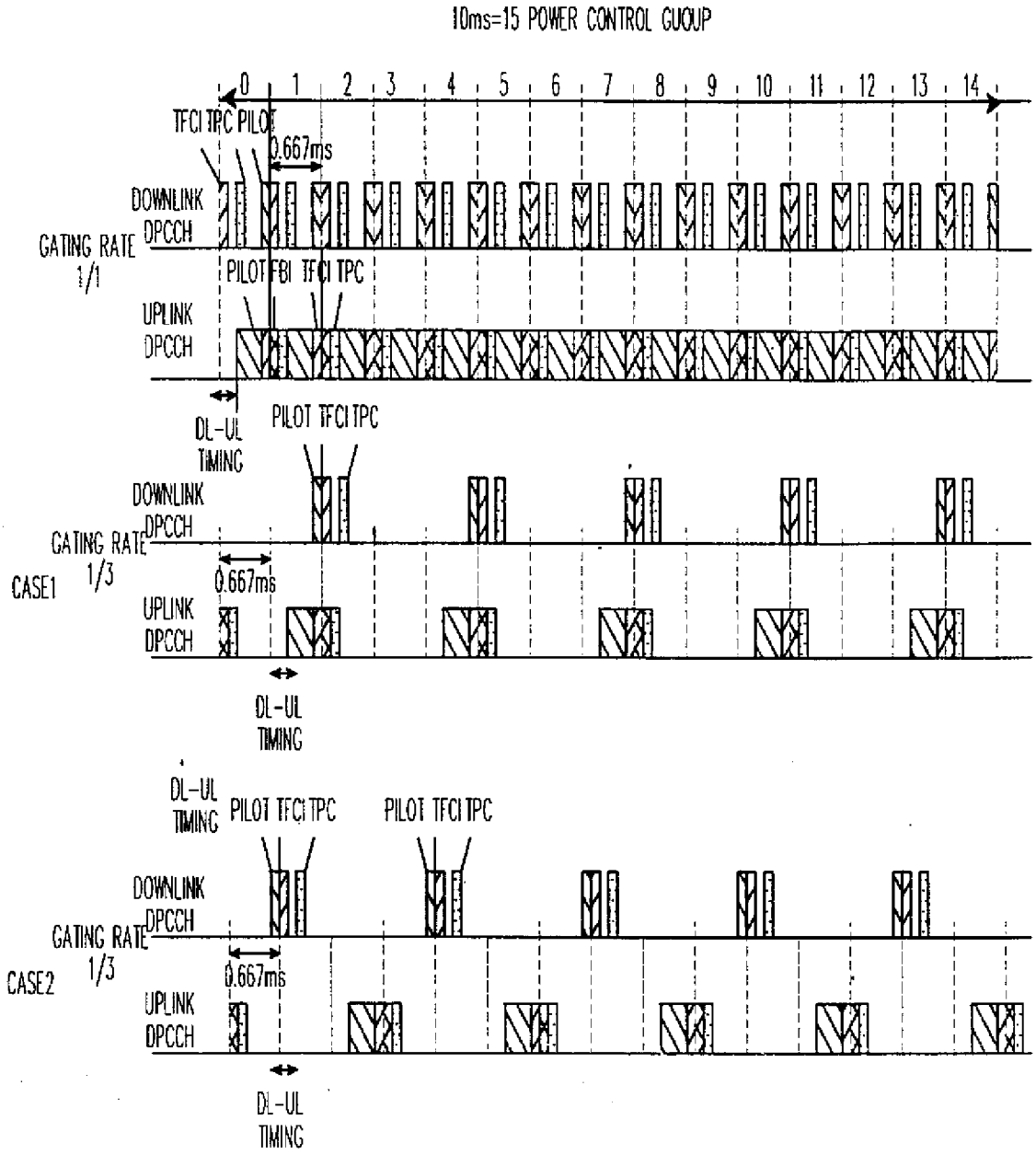

10ms=15 POWER CONTROL GUOUP
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
TFCI TPC PILOT
0.667ms
DOWNLINK DPCCH
GATING RATE 1/1
PILOT FBI TFCI TPC
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/3
CASE1
0.667ms
UPLINK DPCCH
DL-UL TIMING
DL-UL TIMING
PILOT TFCI TPC
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/3
CASE2
0.667ms
UPLINK DPCCH
DL-UL TIMING

FIG. 12A

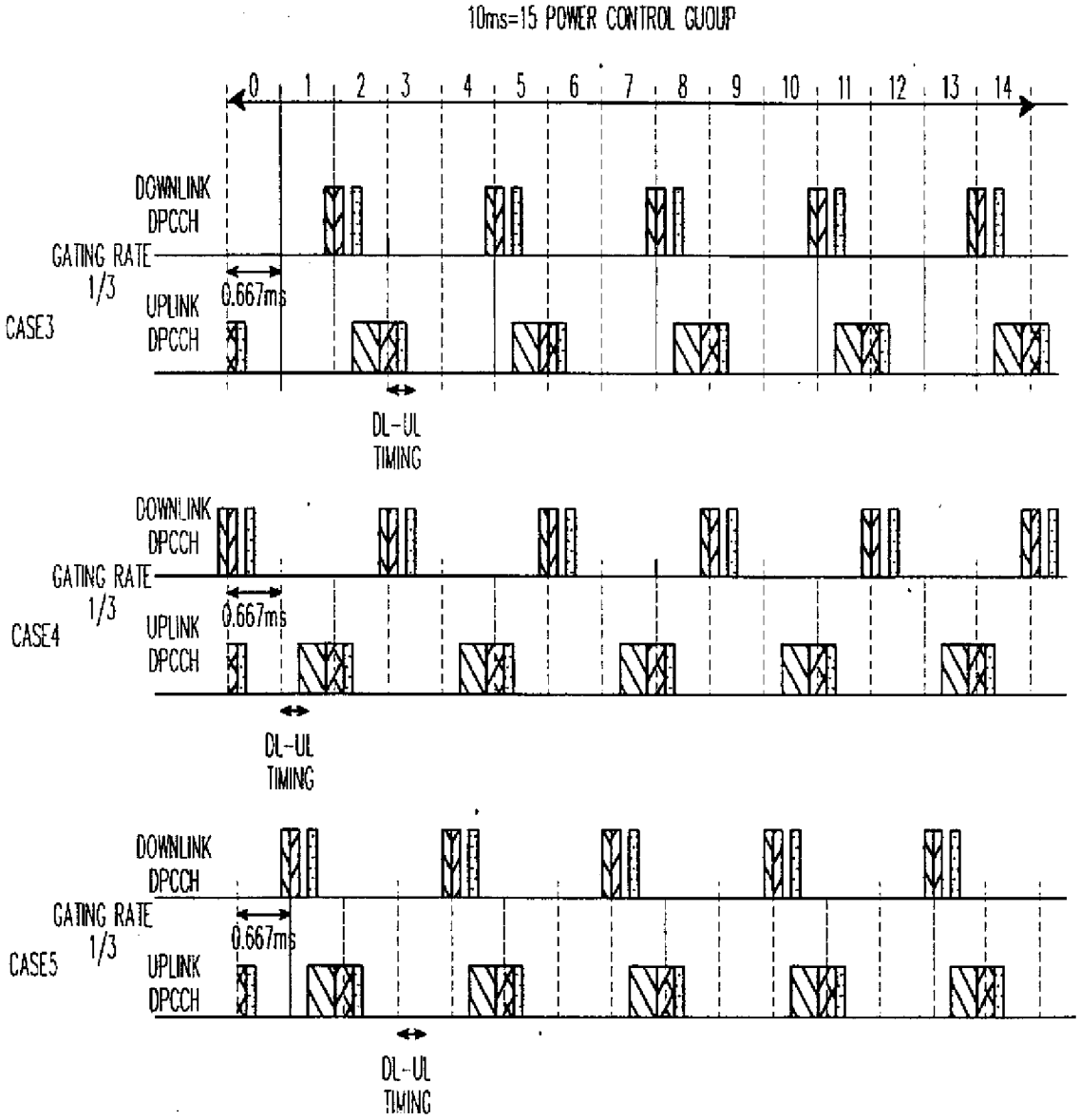

10ms=15 POWER CONTROL GUOUP
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
DOWNLINK DPCCH
GATING RATE 1/3
0.667ms
UPLINK DPCCH
CASE3
DL-UL TIMING
DOWNLINK DPCCH
GATING RATE 1/3
0.667ms
UPLINK DPCCH
CASE4
DL-UL TIMING
DOWNLINK DPCCH
GATING RATE 1/3
0.667ms
UPLINK DPCCH
CASE5
DL-UL TIMING

FIG. 12A

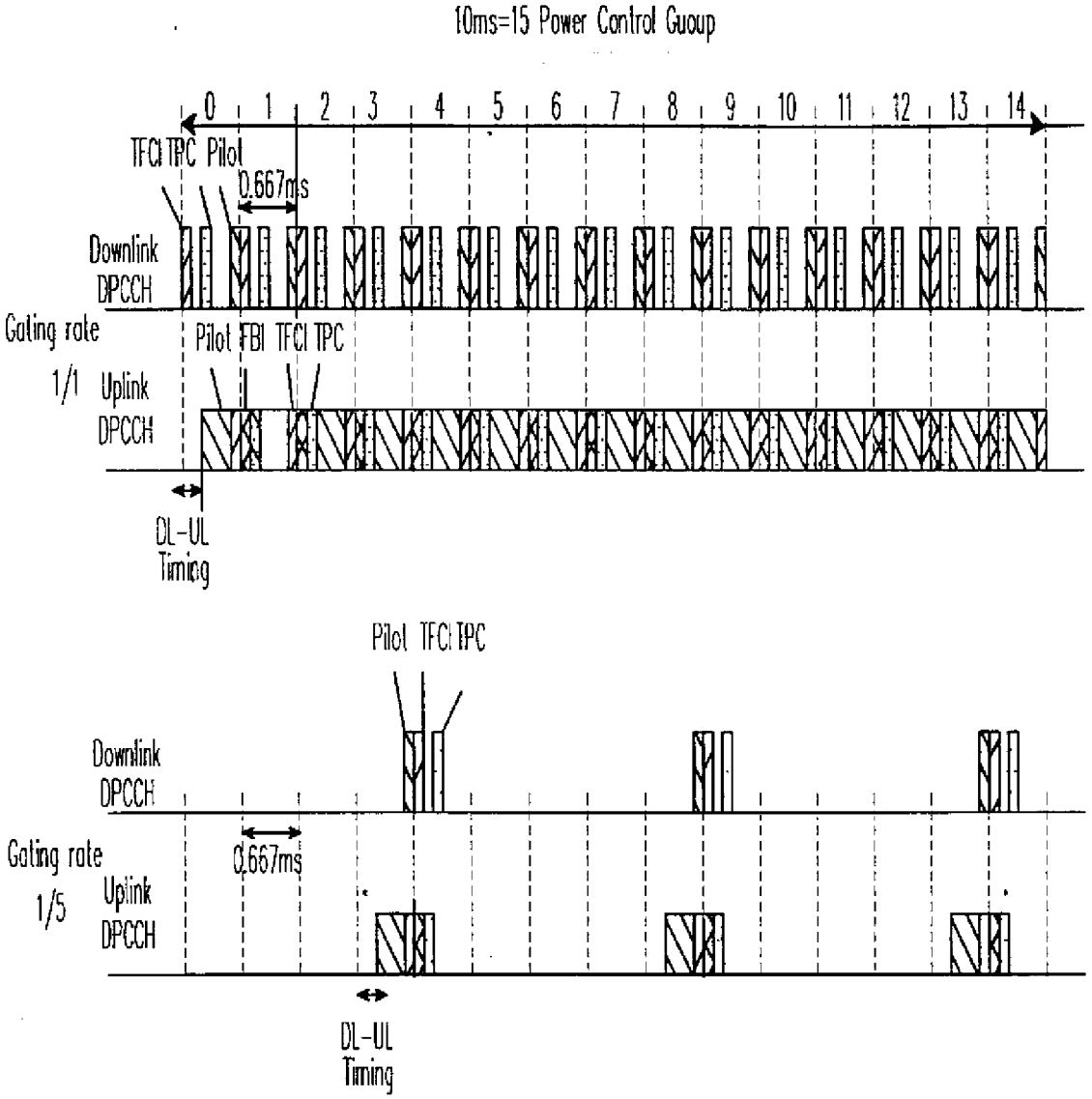

10ms=15 Power Control Guoup
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
TFCI TPC Pilot
0.667ms
Downlink DPCCH
Gating rate 1/1
Pilot FBI TFCI TPC
Uplink DPCCH
DL-UL Timing
Pilot TFCI TPC
Downlink DPCCH
Gating rate 1/5
0.667ms
Uplink DPCCH
DL-UL Timing

FIG. 12B

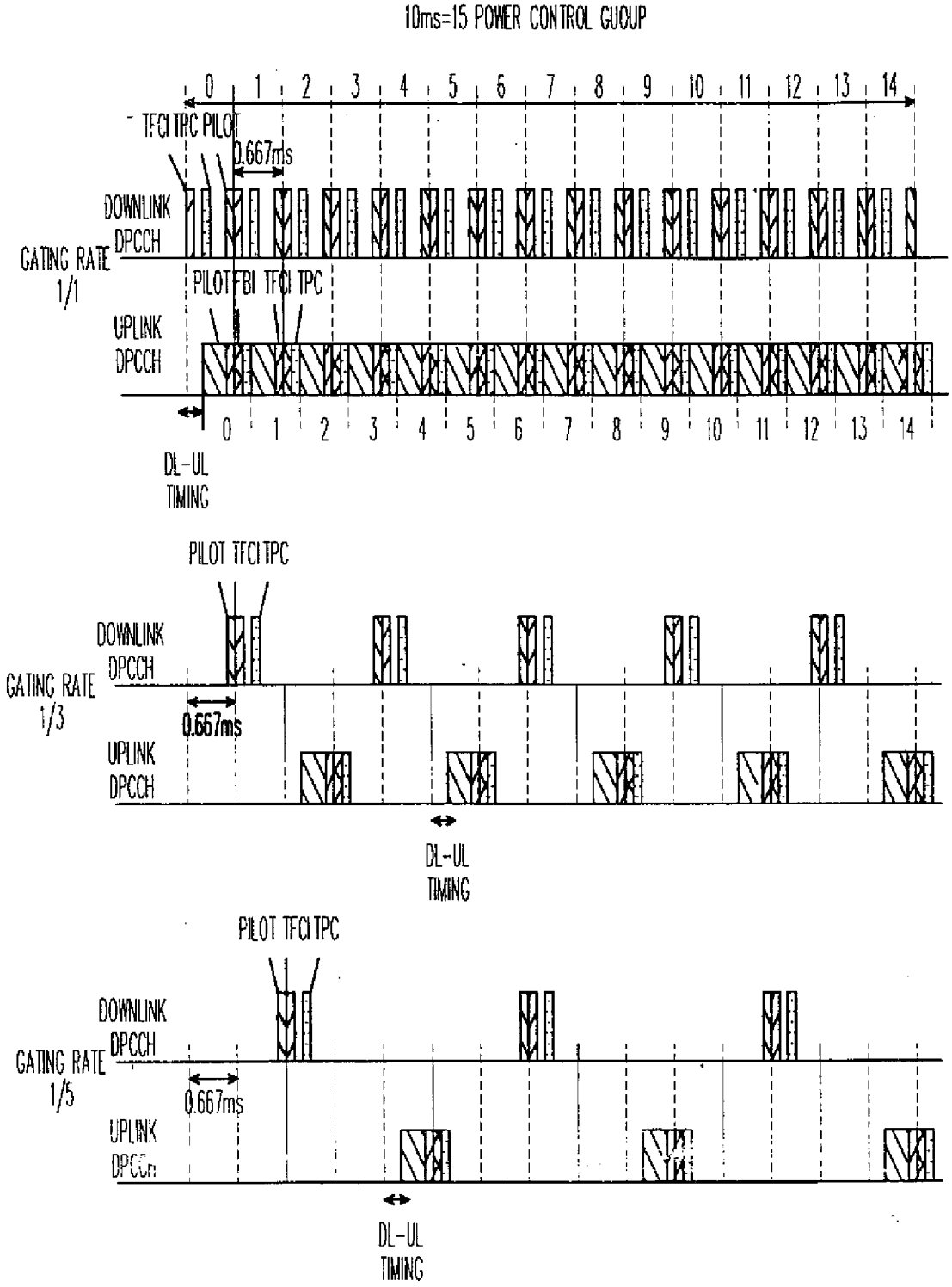

10ms=15 POWER CONTROL GUOUP
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
TFCI TPC PILOT
0.667ms
DOWNLINK DPCCH
GATING RATE 1/1
PILOT FBI TFCI TPC
UPLINK DPCCH
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/3
0.667ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/5
0.667ms
UPLINK DPCCH
DL-UL TIMING

FIG. 12C

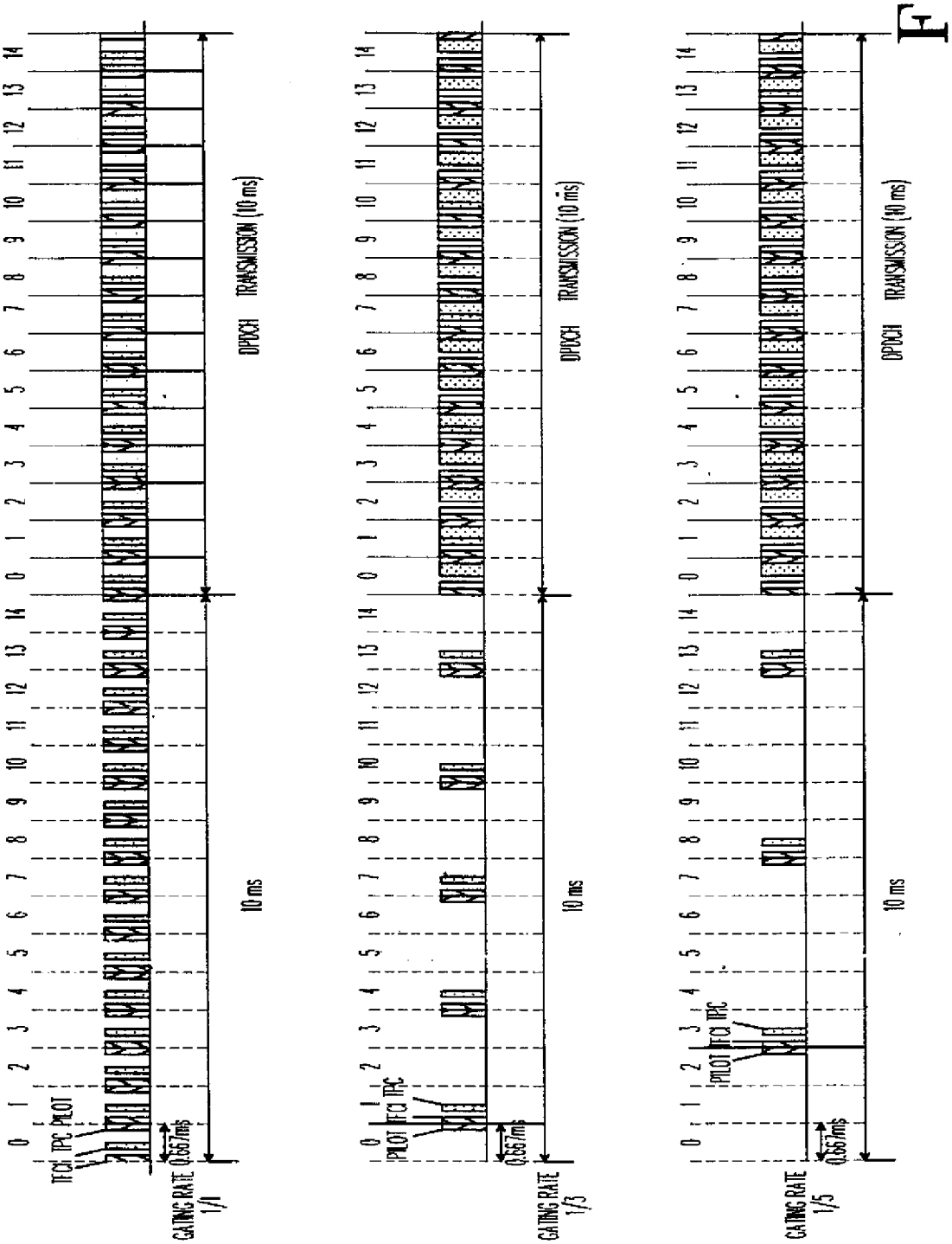

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
TFCI TPC PILOT
0.667ms
GATING RATE 1/1
10 ms
DPDCH TRANSMISSION (10 ms)
PILOT TFCI TPC
0.667ms
GATING RATE 1/3
10 ms
DPDCH TRANSMISSION (10 ms)
PILOT TFCI TPC
0.667ms
GATING RATE 1/5
10 ms
DPDCH TRANSMISSION (10 ms)

FIG. 12D

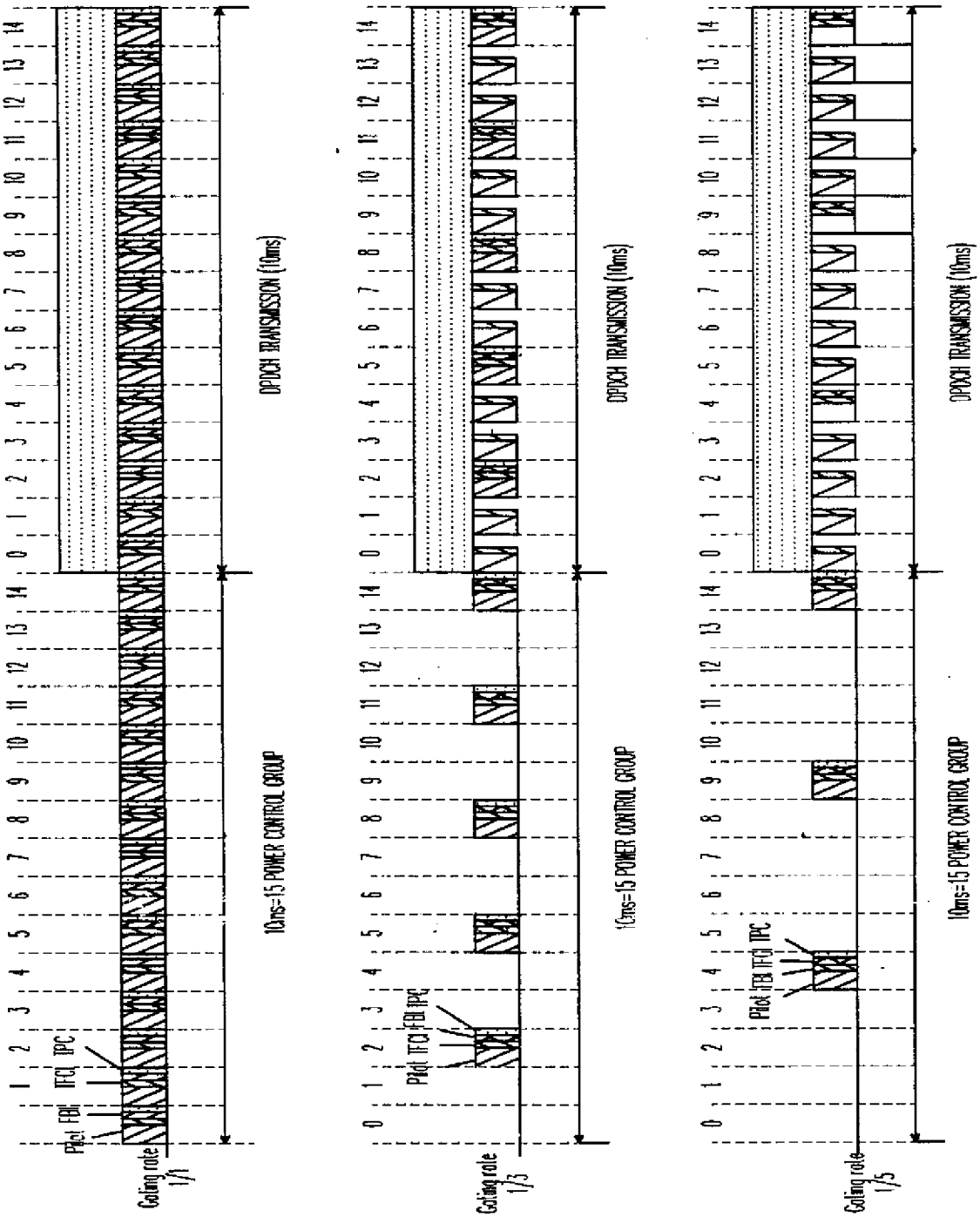

Pilot FBI TFCI TPC
Coding rate 1/1
10ms=15 POWER CONTROL GROUP
0PDCH TRANSMISSION (10ms)
Pilot TFCI FBI TPC
Coding rate 1/3
10ms=15 POWER CONTROL GROUP
0PDCH TRANSMISSION (10ms)
Pilot FBI TFCI TPC
Coding rate 1/5
10ms=15 POWER CONTROL GROUP
0PDCH TRANSMISSION (10ms)

FIG. 12E

INTERNATIONAL SEARCH REPORT

international application No.
PCT/KR00/00345

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H04J 13/00, H04Q 7/30, H04B 7/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimun documentation searched (classification system followed by classification symbols)

Documentation searched other than minimun documentation to the extent that such documents are included in the fileds searched

KR, JP, EP, US ; classes as above

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search trerms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4787095 A (Advanced Micro Device) 22 November 1988	1-5, 7, 8-12, 14, 17-20, 24-27
Y	JP 9-121187 A (NTT) 5. June 1997	1
Y	JP 6-268575 A (FUJITSU) 9. September 1994	2-5, 7, 8-12, 14, 17-20, 24-27
Y	JP 6-350547 A (HITACHI) 22. December 1994	8-10
A	US 5212685 A(IBM) 18 May 1993	1-27

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevence; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevence; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 AUGUST 2000 (02.08.2000)	04 AUGUST 2000 (04.08.2000)

Name and mailing address of the ISA/KR	Authorized officer
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Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-5674

Form PCT/ISA/210 (second sheet) (July 1998)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 April 2001 (12.04.2001)

PCT

(10) International Publication Number
WO 01/26269 A1

(51) Internationaal Patent Classification[7]: H04J 13/00, H04B 1/69

(21) International Application Number: PCT/KR00/01100

(22) International Filing Date: 2 October 2000 (02.10.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

1999/43128	2 October 1999 (02.10.1999)	KR
1999/44627	14 October 1999 (14.10.1999)	KR
1999/45450	15 October 1999 (15.10.1999)	KR
1999/53187	26 November 1999 (26.11.1999)	KR
2000/28775	23 May 2000 (23.05.2000)	KR

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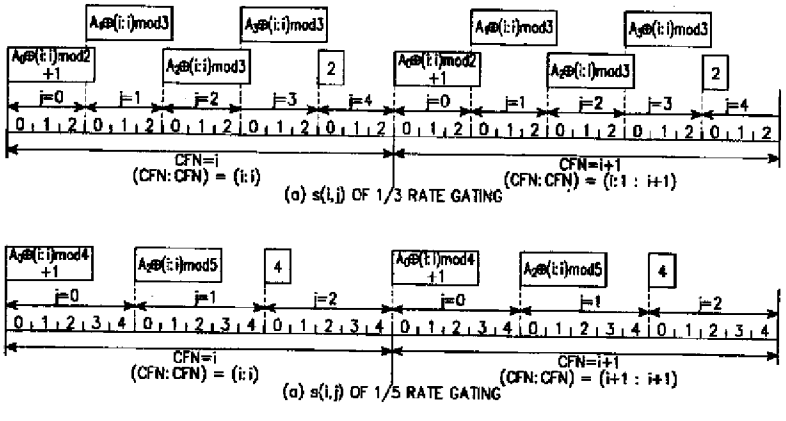
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

[Continued on next page]

(54) Title: APPARATUS AND METHOD FOR GATING DATA ON A CONTROL CHANNEL IN A CDMA COMMUNICATION SYSTEM



(57) Abstract: A method for transmitting control data on a downlink and/or uplink channel in a base station and/or mobile station in a mobile communication system. In one embodiment, the base station determines whether there is downlink channel data to transmit to a mobile station. If there is no data to be transmitted over the downlink channel for a predetermined time period, the base station drives a random gating position selector to determine a random gating slot position, gates on the control data at the determined slot position, and gates off the control data at other slot positions. The random position selector determines the gating slot position by calculating a value x by multiplying a system frame number (SFN) of a received signal by a specific integer; selecting n bits starting from a position which is at an x-chip distance from the start point of a scrambling code, which has a period equal to one frame, before a plurality of gating durations used in generating a downlink signal; and determining a gating slot position of a corresponding gating slot group by performing a modulo operation on the selected n bits, where the module operation is by the number of slots in a gating slot group.

WO 01/26269 A1

(84) **Designated States** *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

— *With international search report.*

APPARATUS AND METHOD FOR GATING DATA ON A CONTROL CHANNEL IN A CDMA COMMUNICATION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a data communication apparatus and method for a CDMA communication system, and in particular, to an apparatus and method for gating data according to whether there is data to transmit.

2. Description of the Related Art

Conventional CDMA (Code Division Multiple Access) mobile communication systems primarily provide voice service. However, future CDMA mobile communication systems will support the IMT-2000 standard, which can provide high-speed data service as well as voice service. More specifically, the IMT-2000 standard can provide high-quality voice service, moving picture service, Internet search service, etc. During data service, IMT-2000 mobile communication systems transmits traffic data over a data channel and transmits control data over a control channel in serial or in parallel with the traffic data. Here, "traffic data" includes voice, picture and packet data, and "control data" includes control and signaling data related to transmission of the traffic data.

In a mobile communication system, data communication is typically characterized by bursts of data transmissions alternating with long periods of non-transmission. The bursts of data are referred to as "packets" or "packages" of data. In the conventional mobile communication system, the base station and the mobile station continuously transmit data on the control channel for a predefined time even when there is no traffic data to transmit. That is, the base station and the mobile station continuously transmit data on the control channel even for the time period where there is no traffic data to transmit, even though this has a deleterious effect on the limited radio resources, base station capacity, power consumption of the mobile station, and interference. This continuous transmission is done in order to minimize the time delay due to sync reacquisition when there is new traffic data to transmit. If there is no data to transmit for a predefined time, the base station and the mobile

station release the data channel and the control channel. In this state, if there is new data to transmit, the base station and the mobile station establish new data channel and control channel.

The IMT-2000 mobile communication system standard defines many states according to channel assignment circumstances and state information existence/nonexistence in order to provide packet data service as well as voice service. For example, a state transition diagram for a cell connected state, a radio bearer activated substate (or RBA mode) and a radio bearer suspended substate (or RBS mode) are well defined in 3GPP RAN TS S2 series S2.03, 99. 04.

FIG. 1A shows state transition in the cell connected state of the conventional mobile communication system. Referring to FIG. 1A, the cell connected state includes a paging channel (PCH) state, a random access channel (RACH)/downlink shared channel (DSCH) state, a RACH/forward link access channel (FACH) state, and a dedicated channel (DCH)/DCH(Dedicated Channel), DCH/DCH+DSCH, DCH/DSCH+DSCH Ctrl (Control Channel) state.

FIG. 1B shows a radio bearer activated substate (i.e., RBA mode) and a radio bearer suspended substate (i.e., RBS mode) within the DCH/DCH, DCH/DCH+DSCH, DCH/DSCH+DSCH Ctrl state.

In many cases, data transmission is performed intermittently, such as for Internet access and file downloading. Therefore, there occurs a non-transmission period between transmissions of packet data. During this period, the conventional data transmission method releases or continuously maintains the data channel. If the dedicated data channel is released, reconnecting the channel requires a long period of time, making it difficult to provide a corresponding service in real time. On the other hand, if the dedicated data channel is maintained, channel resources are wasted.

The downlink (or forward link), which transmits signals from the base station to the mobile station, includes the following physical channels. Physical channels which depart from the scope of the invention will not be described for the sake of simplicity. The downlink physical channels involved in the invention include a dedicated physical control channel (hereinafter, referred to as DPCCH) in which pilot symbols are included for sync acquisition and channel estimation, a dedicated

physical data channel (hereinafter, referred to as DPDCH) for exchanging traffic data with a specific mobile station, and a down link shared channel(DSCH) for transmitting traffic data to multiple mobile stations. The downlink DPDCH includes the traffic data, and the downlink DPCCH includes, at each slot, the control data such as transport format combination indicator (hereinafter, referred to as TFCI), transmit power control (hereinafter, referred to as TPC) information and pilot symbols, which are time multiplexed within one slot. The uplink (or reverse link), which transmits signals from the mobile station to the base station, also has an uplink dedicated control channel and dedicated data channel.

Embodiments of the present invention will be described with reference to the case where the frame length is 10msec and each frame includes 16 slots, i.e., each slot has a length of 0.625msec. Alternatively, embodiments of the present invention will also be described with reference to another case where the frame length is 10msec and each frame includes 15 slots, i.e., each slot has a length of 0.667msec. The slot may have either the same length as a power control group (PCG) or a different length from the power control group. It will be assumed herein that the power control group (0.625msec or 0.667msec) has the same time period as the slot (0.625msec or 0.667msec). The slot includes pilot symbol, traffic data, transport format combination indicator, and power control command bit. The values stated above are given by way of example only.

FIG. 2A shows a slot structure including the downlink DPDCH and DPCCH. In FIG 2A, although the DPDCH is divided into traffic data 1 (Data1) and traffic data 2 (Data2), there is a case where traffic data 1 does not exist and only traffic data 2 exists according to the types of the traffic data. In FIG. 2A, the DPCCH is constructed in the order of TFCI, TPC, and PILOT. Table 1 below shows the symbols constituting the downlink DPDCH/DPCCH fields, wherein the number of TFCI, TPC and pilot bits in each slot can vary according to a data rate and a spreading factor (SF).

Unlike the downlink DPDCH and DPCCH, uplink DPDCH and DPCCH for transmitting signals from the mobile station to the base station are separated by independent channel separation codes.

FIG. 2B shows a slot structure including the uplink DPDCH and DPCCH,

wherein reference numeral 211 indicates a slot structure of the DPDCH and reference numeral 213 indicates a slot structure of the DPCCH. In FIG. 2B, with regard to the DPCCH, the number of TFCI, TPC and pilot bits can vary according to the service option (including the type of the traffic data and the transmit antenna diversity) or a handover circumstance. Tables 2 and 3 below show the symbols constituting the uplink DPDCH and DPCCH fields, respectively.

[Table 1] Downlink DPDCH/DPCCH Fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/Frame			Bits/Slot	DPDCH Bits/Slot		DPCCH Bits/Slot		
			DPDCH	DPCCH	TOT		N_{data1}	N_{data2}	N_{TFCI}	N_{TPC}	N_{pilot}
16	8	512	64	96	160	10	2	2	0	2	4
16	8	512	32	128	160	10	0	2	2	2	4
32	16	256	160	160	320	20	2	8	0	2	8
32	16	256	128	192	320	20	0	8	2	2	8
64	32	128	480	160	640	40	6	24	0	2	8
64	32	128	448	192	640	40	4	24	2	2	8
128	64	64	1120	160	1280	80	14	56	0	2	8
128	64	64	992	288	1280	80	6	56	8	2	8
256	128	32	2400	160	2560	160	30	120	0	2	8
256	128	32	2272	288	2560	160	22	120	8	2	8
512	256	16	4832	288	5120	320	62	240	0	2	16
512	256	16	4704	416	5120	320	54	240	8	2	16
1024	512	8	9952	288	10240	640	126	496	0	2	16
1024	512	8	9824	416	10240	640	118	496	8	2	16
2048	1024	4	20192	288	20480	1280	254	1008	0	2	16
2048	1024	4	20064	416	20480	1280	246	1008	8	2	16

[Table 2] Uplink DPDCH Fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/Frame	Bits/Slot	N_{data}
16	16	256	160	10	10
32	32	128	320	20	20
64	64	64	640	40	40
128	128	32	1280	80	80
256	256	16	2560	160	160
512	512	8	5120	320	320
1024	1024	4	10240	640	640

[Table 3] Uplink DPCCH Fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/Frame	Bits/Slot	N_{pilot}	N_{TPC}	N_{TFCI}	N_{FBI}
16	16	256	160	10	6	2	2	0
16	16	256	160	10	8	2	0	0

16	16	256	160	10	5	2	2	1
16	16	256	160	10	7	2	0	1
16	16	256	160	10	6	2	0	2
16	16	256	160	10	5	1	2	2

Tables 1 to 3 show an example where there exists one DPDCH which is a traffic channel. However, there may exist second, third and fourth DPDCHs according to the service types. Further, the downlink and uplink both may include several DPDCHs. Although the base station transmitter and the mobile station transmitter will be described with reference to the case where there exist three DPDCHs, the number of DPDCHs is not limited.

FIG. 3A shows a structure of the conventional base station transmitter. Referring to FIG. 3A, multipliers 111, 121, 131 and 132 multiply outputs of DPCCH, $DPDCH_1$(or DSCH), $DPDCH_2$ and $DPDCH_3$ data generators 101, 102, 103 and 104, which have undergone channel encoding and interleaving, by their associated gain coefficients G_1, G_2, G_3 and G_4, respectively. The gain coefficients G_1, G_2, G_3 and G_4 may have different values according to circumstances such as the service option and the handover. A multiplexer (MUX) 112 time-multiplexes the DPCCH signal and the $DPDCH_1$ signal into the slot structure of FIG. 2A. A first serial-to-parallel (S/P) converter 113 distributes the output of the multiplexer 112 to an I channel and a Q channel. Second and third S/P converters 133 and 134 S/P-convert the $DPDCH_2$ and $DPDCH_3$ signals and distribute them to the I channel and the Q channel, respectively.

The S/P-converted I and Q channel signals are multiplied by channelization codes C_{ch1}, C_{ch2} and C_{ch3} in multipliers 114, 122, 135, 136, 137 and 138, for spreading and channel separation. Orthogonal codes are used for the channelization codes. The I and Q channel signals multiplied by the channelization codes in the multipliers 114, 122, 135, 136, 137 and 138 are summed by first and second summers 115 and 123, respectively. That is, the I channel signals are summed by the first summer 115, and the Q channel signals are summed by the second summer 123. The output of the second summer 123 is phase shifted by 90° by a phase shifter 124. A summer 116 sums an output of the first summer 115 and an output of the phase shifter 124 to generate a complex signal I+jQ. A multiplier 117 scrambles the complex signal with a PN sequence C_{scramb} which is uniquely assigned to each base station, and a signal separator 118 separates the scrambled signal into a real part and an imaginary part and distributes them to the I channel and the Q channel. The I and Q channel outputs

of the signal separator 118 are filtered by lowpass filters 119 and 125, respectively, to generate bandwidth-limited signals. The output signals of the filters 119 and 125 are multiplied by carriers $\cos\{2\pi f_c t\}$ and $\sin\{2\pi f_c t\}$ in multipliers 120 and 126, respectively, to frequency-up convert the signals to a radio frequency (RF) band. A adder 127 sums the frequency-shifted I and Q channel signals.

FIG. 3B shows a structure of the conventional mobile station transmitter. Referring to FIG. 3B, multipliers 211, 221, 223 and 225 multiply outputs of DPCCH, $DPDCH_1$, $DPDCH_2$ and $DPDCH_3$ data generators 201, 202, 203 and 204, which have undergone channel encoding and interleaving, by their associated channelization codes C_{ch1}, C_{ch2}, C_{ch3} and C_{ch4}, respectively, for spreading and channel separation. Orthogonal codes are used for the channelization codes. The output signals of the multipliers 211, 221, 223 and 225 are multiplied by their associated gain coefficients G_1, G_2, G_3 and G_4 in multipliers 212, 222, 224 and 226, respectively. The gain coefficients G_1, G_2, G_3 and G_4 may have different values.

The outputs of the multipliers 212 and 222 are summed by a first summer 213 and output as an I channel signal, and the outputs of the multipliers 224 and 226 are summed by a second summer 227 and output as a Q channel signal. The Q channel signal output from the second summer 227 is phase shifted by 90° in a phase shifter 228. A summer 214 sums the output of the first summer 213 and the output of the phase shifter 228 to generate a complex signal I+jQ. A multiplier 215 scrambles the complex signal with a PN sequence C_{scramb} which is uniquely assigned to the mobile station, and a signal separator 229 separates the scrambled signal into a real part and an imaginary part and distributes them to the I channel and the Q channel. The I and Q channel outputs of the signal separator 229 are filtered by lowpass filters 216 and 230, respectively, to generate bandwidth-limited signals. The output signals of the filters 216 and 230 are multiplied by carriers $\cos\{2\pi f_c t\}$ and $\sin\{2\pi f_c t\}$ in multipliers 217 and 231, respectively, to frequency-up convert the signals to a radio frequency (RF) band. A adder 218 sums the frequency-up-converted I and Q channel signals.

FIG. 4A shows a conventional method of transmitting the downlink DPCCH and the uplink DPCCH in the RBS mode when transmission of the uplink DPDCH is discontinued. FIG. 4B shows a conventional method of transmitting the downlink

DPCCH and the uplink DPCCH in the RBS mode when transmission of the downlink DPDCH is discontinued.

As illustrated in FIGS. 4A and 4B, the mobile station constantly transmits the uplink DPCCH in the RBS mode in order to avoid a resynchronization acquisition process in the base station. When there is no traffic data to transmit for a long time in the RBS mode, the base station and the mobile station make a transition to an RRC (Radio Resource Control) connection released state. In this state, transmission of the uplink DPDCH is discontinued, but the mobile station transmits pilot symbols and TPC (Transmit Power Control) bits over the DPCCH until the transition is completed, thereby there is an unnecessary interference in the uplink. The interference of the uplink causes a decrease in the capacity of the uplink.

In the conventional method, although continuous transmission of the uplink DPCCH is advantageous in that it is possible to avoid the sync reacquisition process in the base station, it increases interference to the uplink, causing a decrease in the capacity of the uplink. Further, in the downlink, continuous transmission of the uplink transmission power control(TPC) bits causes an interference of the downlink and a decrease in the capacity of the downlink. Therefore, it is necessary to minimize the time required for the sync reacquisition process in the base station, to minimize the interference due to transmission of the uplink DPCCH signal and to minimize the interference due to transmission of the uplink transmission power control(TPC) bits over the downlink.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide an apparatus and method for transmitting on and off a DPCCH signal when there is no traffic data(user data or signaling message) to transmit over a data channel for a predefined time in a mobile communication system.

It is another object of the present invention to provide an apparatus and method for gating slot data on the DPCCH in an irregular pattern when there is no traffic data to transmit over the data channel for a predefined time in a mobile communication system.

It is further another object of the present invention to provide an apparatus and method for performing a gated transmission procedure when there is no traffic data to transmit over the data channel for a predefined time, and randomly gating a given slot in a gating slot group unit set during the gated transmission procedure, in a mobile communication system.

It is yet another object of the present invention to provide an apparatus and method in which a base station performs a gated transmission procedure when there is no traffic data to transmit over the data channel for a predefined time, and randomly gates a given slot in a gating slot group unit set during the gated transmission procedure, in a mobile communication system.

It is still another object of the present invention to provide an apparatus and method in which a mobile station performs a gated transmission procedure upon receipt of a message for performing the gated transmission procedure from a base station, and randomly gates a given slot in a gating slot group unit set during the gated transmission procedure, in a mobile communication system.

It is still another object of the present invention to provide an apparatus and method for performing a gated transmission procedure when there is no traffic data to transmit over the data channel for a predefined time, and randomly gating a given slot in a gating slot group unit set as a connected frame number during the gated transmission procedure, in a mobile communication system.

It is still another object of the present invention to provide an apparatus and method for gating slot data on a DPCCH by transmitting a pilot symbol of a slot located before gated on slot and transmitting TFCI and TPC of the gated on slot, in a mobile communication system.

It is still another object of the present invention to provide an apparatus and method for controlling transmission power of control data using power control information while gating data on the DPCCH, in a mobile communication system.

To achieve the above and other objects, there is provided a method for transmitting control data on a downlink channel in a base station for a mobile communication system. The base station determines whether there is downlink data

channel data to transmit to a mobile station. If there is no data to be transmitted over the downlink data channel(DCH or DSCH) for a predetermined time, the base station drives a random position selector to determine a gating slot position, gating on the control data in the determined slot position, and gating off the control data in other positions. All channel data is organized into a stream of frames, each frame includes a plurality of slots, the slots in each frame are divided into a plurality of gating slot groups, and the determined slot position is a randomized slot position in each gating slot group.

Preferably, the random position selector determines the gating slot position by calculating a value x by multiplying a system frame number (SFN) of a received signal by a specific integer; selecting n bits in a position which is at an x-chip distance from a start point of a corresponding Gold code before a plurality of gating durations used in generating a downlink signal; and determining a gating slot position of a corresponding gating slot group by performing a modulo operation by the number of the slots constituting the gating slot group on the selected bits.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings in which:

FIG. 1A is a conventional state transition diagram for a packet data service;

FIG. 1B is a conventional state transition diagram between a RBA mode and a RBS mode of the DCH/DCH state;

FIG. 2A is a diagram illustrating a slot structure of downlink DPDCH and DPCCH in a CDMA communication system;

FIG. 2B is a diagram illustrating a slot structure of uplink DPDCH and DPCCH in a CDMA communication system;

FIG. 3A is a diagram illustrating a structure of a conventional base station transmitter in a CDMA communication system;

FIG. 3B is a diagram illustrating a structure of a conventional mobile station transmitter in a CDMA communication system;

FIG. 4A is a diagram illustrating a conventional method of transmitting a downlink DPCCH and an uplink DPCCH when transmission of an uplink DPDCH is discontinued in the RBS mode in a CDMA communication system;

FIG. 4B is a diagram illustrating a conventional method of transmitting the downlink DPCCH and the uplink DPCCH when transmission of a downlink DPDCH is discontinued in the RBS mode in a CDMA communication system;

FIG. 5A is a diagram illustrating a structure of a base station transmitter for gating data on the DPCCH according to an embodiment of the present invention;

FIG. 5B is a diagram illustrating a structure of a mobile station transmitter for gating data on the DPDCH according to an embodiment of the present invention;

FIG. 5C is a diagram illustrating a structure of a base station transmitter with a gating position selector, for gating data on the DPDCH according to an embodiment of the present invention;

FIG. 5D is a diagram illustrating a structure of a mobile station transmitter with a gating position selector, for gating data on the DPDCH according to an embodiment of the present invention;

FIG. 6A is a diagram illustrating a method for transmitting a signal according to a regular or gated transmission pattern for an uplink DPCCH in the RBS mode according to an embodiment of the present invention;

FIG. 6B is a diagram illustrating another method for transmitting a signal according to a regular or gated transmission pattern for an uplink DPCCH in the RBS mode according to an embodiment of the present invention;

FIG. 7A is a diagram illustrating a method for transmitting a signal when an uplink DPDCH message is generated while gating an uplink DPCCH in the RBS mode according to an embodiment of the present invention;

FIG. 7B is a diagram illustrating another method for transmitting a signal when an uplink DPDCH message is generated while gating an uplink DPCCH in the RBS mode according to an embodiment of the present invention;

FIG. 8A is a diagram illustrating a method for transmitting downlink and uplink signals when transmission of a downlink DPDCH is discontinued according to an embodiment of the present invention;

FIG. 8B is a diagram illustrating a method for transmitting downlink and uplink signals when transmission of an uplink DPDCH is discontinued according to an embodiment of the present invention;

FIG. 8C is a diagram illustrating another method for transmitting downlink and uplink signals when transmission of the downlink DPDCH is discontinued according to an embodiment of the present invention;

FIG. 8D is a diagram illustrating another method for transmitting downlink and uplink signals when transmission of the uplink DPDCH is discontinued

according to an embodiment of the present invention;

FIG. 9A is a diagram illustrating a method for transmitting downlink and uplink signals when transmission of a downlink DPDCH is discontinued (gated transmission for the downlink DPCCH) according to an embodiment of the present invention;

FIG. 9B is a diagram illustrating a method for transmitting downlink and uplink signals when transmission of an uplink DPDCH is discontinued (gated transmission for downlink DPCCH) according to an embodiment of the present invention;

FIG. 10A is a diagram illustrating a structure of a base station transmitter according to another embodiment of the present invention;

FIG. 10B is a diagram illustrating a structure of a mobile station transmitter according to another embodiment of the present invention;

FIG. 11A is a diagram illustrating gated transmission for downlink and uplink DPCCHs according to a first embodiment of the present invention;

FIG. 11B is a diagram illustrating gated transmission for downlink and uplink DPCCHs according to a second embodiment of the present invention;

FIG. 11C is a diagram illustrating gated transmission for downlink and uplink DPCCHs according to a third embodiment of the present invention;

FIG. 11D is a diagram illustrating gated transmission for downlink and uplink DPCCHs according to a fourth embodiment of the present invention;

FIGS. 12A and 12B are diagrams illustrating gated transmission for downlink and uplink DPCCHs according to a fifth embodiment of the present invention;

FIG. 12C is a diagram illustrating gated transmission for downlink and uplink DPCCHs according to a sixth embodiment of the present invention;

FIG. 12D is a diagram illustrating gated transmission for downlink and uplink DPCCHs according to a seventh embodiment of the present invention;

FIG. 12E is a diagram illustrating gated transmission for downlink and uplink DPCCHs according to an eighth embodiment of the present invention;

FIG. 13A is a diagram illustrating a method for determining a position selection bit during gated transmission of the downlink and uplink DPCCHs according to the first embodiment of the present invention;

FIG. 13B is a diagram illustrating a method for determining a position selection bit during gated transmission of the downlink and uplink DPCCHs according to the second embodiment of the present invention;

FIG. 13C is a diagram illustrating a method for determining a position selection bit during gated transmission of the downlink and uplink DPCCHs according to the third embodiment of the present invention;

FIG. 13D is a diagram illustrating a method for determining a position selection bit during gated transmission of the downlink and uplink DPCCHs according to the fourth embodiment of the present invention;

FIG. 14A is a diagram illustrating gated transmission for downlink and uplink DPCCHs according to a ninth embodiment of the present invention;

FIG. 14B is a diagram illustrating gated transmission for downlink and uplink DPCCHs according to a tenth embodiment of the present invention;

FIG. 14C is a diagram illustrating gated transmission for downlink and uplink DPCCHs according to an eleventh embodiment of the present invention;

FIG. 14D is a diagram illustrating gated transmission for downlink and uplink DPCCHs according to a twelfth embodiment of the present invention;

FIG. 15A is a diagram illustrating a method for extracting a partial sequence required to generate a gated transmission pattern from an uplink scrambling code according to an embodiment of the present invention;

FIG. 15B is a diagram illustrating a method for extracting an n-bit sequence required to generate a gated transmission pattern from a fixed sequence according to an embodiment of the present invention;

FIG. 16 is a diagram illustrating a structure of a gating position selector for selecting a gating position by using the uplink scrambling code of FIG. 15A and the fixed sequence of FIG. 15B together with CFN according to an embodiment of the present invention;

FIG. 17A is a diagram illustrating a power control time relationship when 1/3 rate gating is applied to both the downlink and the uplink according to an embodiment of the present invention;

FIG. 17B is a diagram illustrating a power control time relationship when 1/5 rate gating is applied to both the downlink and the uplink according to an embodiment of the present invention;

FIG. 18A is a diagram illustrating a power control time relationship when 1/3 rate gating is applied to only the downlink according to an embodiment of the present invention; and

FIG. 18B is a diagram illustrating a power control time relationship when 1/5 rate gating is applied to only the downlink according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described herein below with reference to the accompanying drawings. In the following description, well-known functions or constructions are not described in detail since they would obscure the invention in unnecessary detail.

The term "normal transmission" as used herein refers to continuously transmitting TFCI, TPC and pilot symbol included in the downlink or uplink DPCCH. Further, the term "gated transmission" refers to transmitting TFCI, TPC and pilot symbol included in the downlink or uplink DPCCH, only at a specific power control group (or slot) according to a predetermined pattern, or refer to gated on transmission of a DPCCH signal only at a pilot symbol of a slot located before gated on slot and TFCI and TPC of the gated on slot according to a predetermined gated on pattern. The information, transmission of which is discontinued in the downlink DPCCH during gated transmission, may include either all or some of the TFCI, TPC and pilot symbol in one power control group (or slot). In addition, the term "gating position selection" as used herein refers to selecting a position of a slot for transmitting data on the DPCCH during gated transmission, and "gating position" refers to the slot selected for transmitting the control data. Further, the term "control data" as used herein refers to a DPCCH signal, and the term "traffic data" refers to signaling data and/or user data which is transmitted in bursts between the base station and the mobile station. TFCI, TPC, FBI(Feedback Indicator) and pilot symbol are included in the "control data". Although the invention will be described with reference to an example of gating data on the DPCCH, the gated transmission method according to the present invention can also be applied to the case of gating control data on any other channel which periodically transmits control data.

The gated transmission operation, which will be described later, can be applied to either the case when the gated transmission unit is equal to the slot unit, or the case when the gated transmission unit is not equal to the slot unit. When the gated transmission unit is not equal to the slot unit, it is preferable to gate TPC, TFCI and pilot symbol differently. That is, an nth pilot symbol and (n+1)th TFCI and TPC are set as a gated transmission unit.

In addition, since performance at the beginning of a frame is very important, the preferred embodiments of the present invention locate the TPC, which is for controlling the power of the first slot of the next frame, at the last slot of one frame. That is, TPC bits for the downlink DPCCH and the uplink DPCCH are located at the last slot of the nth frame, and power of the first slot of the (n+1)th frame is controlled using the TPC bits existing at the last slot of the nth frame.

In an exemplary embodiment of the present invention, when the mobile communication system performs gated transmission, the base station and the mobile station determine positions of the gating slots according to either a predetermined regular pattern, or an irregular pattern determined by setting given slots in a gating slot group as gating positions using the System Frame Number (SFN) and the Connection Frame Number (CFN). Further, in the mobile communication system, a DPDCH and one frame of the DPDCH can be comprised of a plurality of slots. In the various embodiments of the present invention, one frame can be comprised of 15 or 16 slots, and the invention will be described here for both cases. Below, the gated transmission operation performed in the regular pattern will be described with reference to the case where one frame is comprised of 16 slots, and the gated transmission performed in the irregular pattern will be described with reference to the case where one frame is comprised of 15 slots.

The invention will be described focusing on the process of performing 1/3 and 1/5 rate gated transmission on the downlink and uplink DPCCHs of FIGS. 2A and 2B. It is also possible to determine gating positions according to random patterns as shown in FIGS. 15A, 15B and 16.

A hardware structure according to an embodiment of the invention will be described below.

FIG. 5A shows a structure of a base station transmitter according to an embodiment of the present invention. The base station transmitter is different from the conventional one of FIG. 3A in that with regard to the downlink DPCCH, the output of the multiplier 111 is gated by a gated transmission controller 141. That is, the gated transmission controller 141 performs gated transmission on a pilot symbol of one slot of the downlink DPCCH and TFCI and TPC bits of the next slot in a

pattern scheduled with the mobile station, when the traffic data to be transmitted over the downlink DPDCH is not generated for a predetermined time or when traffic data is not received over the uplink DPDCH for a predetermined time. In addition, the gated transmission controller 141 performs gated transmission on one power control group (or one entire slot) including the pilot symbols, TFCI and TPC bits for the downlink DPCCH at a power control group (or time slot) scheduled with the mobile station in the RBS mode where the traffic data is not transmitted over the downlink and uplink DPDCHs.

When the downlink and uplink DPCCH signals are simultaneously gated, the downlink gating pattern is equal to the uplink gating pattern, but an offset may exist between them for efficient power control. The offset can be given as a system parameter or can be known by a message indicating the start of gated transmission. The gating start indication message is transmitted from the base station to the mobile station to indicate a start point of gated transmission and a gating rate, after traffic data to be transmitted over the DPDCH is not generated for a predetermined time. This message can also be transmitted from the mobile station to the base station. In addition, the base station can determine a gating start indication message in response to a gating request of the mobile station, and transmit the determined message to the mobile station.

The gated transmission controller 141 can gate either the slot data on the DPCCH or the control data of multiple slots. One slot of the DPCCH is comprised of the control data such as pilot symbol, TFCI and TPC (in the mobile station, FBI is further included). During gated transmission, the gated transmission controller 141 can gate the entire control data included in the slot of the gating position. As an alternative method, the gated transmission controller 141 can gate a pilot symbol of an nth slot duration located before an (n+1)th slot of the gating position, and TPC and TFCI bits of the (n+1)th slot. This embodiment of the present invention will be described with reference to the latter method.

In addition, the gated transmission controller 141 locates the TPC bits at the last slot of one frame, where the TPC bits are for power controlling the first slot of the next frame in order to guarantee performance of the beginning part of the next frame. That is, the TPC bits for the downlink DPCCH and the uplink DPCCH are located at the last slot of the nth frame, and power of the first slot of the (n+1)th

frame is controlled using the TPC bits existing at the last slot of the nth frame.

When the mobile station performs gated transmission and the base station does not perform gated transmission, the base station transmitter determines a TPC (Transmit Power Control) bit by measuring the one DPCCH slot signal discontinuously transmitted from the mobile station and then transmits the determined TPC bit at every slot until the base station determines new TPC bit by measuring another up link DPCCH slot signal.

FIG. 5B shows a structure of a mobile station transmitter according to an embodiment of the present invention. The mobile station transmitter is different from the conventional one of FIG. 3B in that a gated transmission controller 241 is provided to gate transmission of the uplink DPCCH. That is, the gated transmission controller 241 performs gated transmission on one power control group (or one entire slot) including the pilot symbols, TFCI, FBI and TPC bits for the uplink DPCCH at a power control group (or time slot) scheduled with the base station, when traffic data to be transmitted over the downlink and uplink data channels(DPDCH or DSCH) is not generated for a predetermined time or when traffic data to be transmitted over the uplink DPDCH is not generated for a predetermined time.

Now, a description will be made of a transmission signal structure of the base station and the mobile station according to an embodiment of the present invention.

FIG. 6A shows a method for transmitting an uplink DPCCH signal according to a regular or gated transmission pattern when there is no data to be transmitted over the DPDCH for a predetermined period of time according to an embodiment of the present invention. In FIG. 6A, reference numerals 301, 302, 303 and 304 show different gating rates according to duty cycles (hereinafter, referred to as DC). Herein, the "duty cycle" (or "DC") and the "gating rate" are used to refer to the same thing. Reference numeral 301 shows a conventional method for transmitting the uplink DPCCH without gating (DC=1), and reference numeral 302 shows a method for regularly transmitting every other power control group (or time slot), when DC=1/2 (only 1/2 of all the slots in one frame are transmitted). Reference numeral 303 shows a method for regularly transmitting every fourth

slot(3rd, 7th, 11th and 15th slots), when DC=1/4 (only 1/4 of all the slots in one frame are transmitted). Reference numeral 304 shows a method for regularly transmitting every eighth slots (7th and 15th slots), when DC=1/8 (only 1/8 of all the slots in one frame are transmitted).

In the embodiment of FIG. 6A, when DC=1/2 and 1/4, although the gated transmission controller 241 of the mobile station regularly gates the slots of the uplink DPCCH, it is also possible to gate arbitrary slots according to the corresponding DC. That is, when DC=1/2, it is also possible to continuously gate adjacent arbitrary slots according to an irregular pattern, rather than regularly transmitting every other slot. Further, when DC=1/2, it is also possible to continuously transmit half of all the slots at the second half (8th to 15th slots) of the frame. When DC=1/4, it is also possible to continuously transmit 1/4 of all the slots beginning at a 3/4 point of the frame (i.e., 12th to 15th slots). When DC=1/8, it is also possible to continuously transmit 1/8 of all the slots beginning at a 7/8 point of the frame (i.e., 14th to 15th slots).

The gating rate can be varied during gated transmission. For this, the mobile station and the base station should know when and which gating rate they will use, so that it is necessary to transmit a message for this. The gating rate is determined at the start of gated transmission and preferably, not changed during the gated transmission.

FIG. 6B shows a method for transmitting a signal according to a regular or gated transmission pattern for the uplink DPCCH according to another embodiment of the present invention. In FIG. 6B, reference numerals 305, 306 and 307 show different gating rates according to a ratio of a duty cycle DC. Reference numeral 305 shows a method for transmitting two consecutive slots at regular locations (2^{nd}-3^{rd}, 6^{th}-7^{th}, 10^{th}-11^{th} and 14^{th}-15^{th} slots), when DC=1/2 (only 1/2 of all the slots in one frame are transmitted). Reference numeral 306 shows a method for transmitting two consecutive slots at regular locations (6^{th}-7^{th} and 14^{th}-15^{th} slots), when DC=1/4 (only 1/4 of all the slots in one frame are transmitted). Reference numeral 307 shows a method for transmitting two consecutive slots at regular locations (14^{th}-15^{th} slots), when DC=1/8 (only 1/8 of all the slots in one frame are transmitted).

In the embodiment of FIG. 6B, when DC=1/2 and 1/4, although the gated

transmission controller 241 of the mobile station regularly gates the slots of the uplink DPCCH, it is also possible to gate arbitrary slots out of all the slots according to the corresponding DC. That is, when DC=1/2, it is also possible to continuously gate 4 consecutive slots (e.g., 2^{nd}-5^{th} slots) according to an irregular pattern, rather than regularly transmitting every other 2 consecutive slots.

Next, a description will be made of signal transmission diagrams of the base station and the mobile station according to another embodiment, in which the slot gating positions are selected such that a signal should be transmitted at one of consecutive three or five consecutive slots. The embodiment will be described for the gating rate of 1/3 or 1/5, in the case where one frame includes 15 slots (i.e. power control groups).

FIG. 5C shows a structure of a base station transmitter with a gating position selector according to an embodiment of the present invention. The base station transmitter is different from that of FIG. 5A in that the positions of the transmission slots for the downlink DPCCH are selected by a gating position selector 142.

FIG. 5D shows a structure of a mobile station transmitter with a gating position selector according to an embodiment of the present invention. The base station transmitter is different from that of FIG. 5B in that the positions of the transmission slots for the uplink DPCCH are selected by a gating position selector 242.

Arranging the gating positions of the slots irregularly is to prevent electromagnetic wave-related bad effects due to the power of the regularly transmitted signals. In this embodiment, a scrambling code is used to irregularly gating the transmission signals.

One method for selecting the gating positions of the gating slot is to use the system frame number (SFN) of a downlink signal immediately before transmission of an uplink signal, and a scrambling code generated to descramble a received downlink signal in the mobile station. The mobile station reads a code bits in a specific position of the scrambling code using the SFN of the downlink signal, and determines the gating slots using the read value. Since the SFN value of 0 to 71 is continuously transmitted over a broadcasting channel from the base station, the

mobile station can read the SFN by receiving data on the broadcasting channel. For the scrambling code, a secondary scrambling code or a primary scrambling code can be used. If the base station knows the gating position of the mobile station, it can exactly receive the data gated-on by the mobile station. Therefore, it is preferable that the gating position should be agreed between the transmission side and the receiving side. For this agreement, this embodiment uses a scrambling code with a random property, which is equally used by the base station and the mobile station, and the SFN for reducing the periodicity, thereby to determine a position of a slot to be gated.

The gating position controller 242(FIG. 5D) of the mobile station determines a position of the slot to be gated on by using a Gold code, which is a real part of a scrambling code generated internally to descramble a received signal, and the SFN of the received signal. When DC=1/3, the gating position controller 242 selects one slot in an arbitrary position out of 3 slots (gating slot group), and when DC=1/5, the gating position controller 242 selects one slot in an arbitrary position out of 5 slots (gating slot group). Herein, the 3-slot duration for DC=1/3 and the 5-slot duration for DC=1/5 will be referred to as "gating duration" or "gating slot group".

A first method for randomly determining the slot to be gated on in a gating slot group unit according to an embodiment of the present invention is determined in the following order. FIGs 13A, 13B, 14A, and 14B are related to this method

1. A system frame number (SFN) 0 to 71 of a signal received immediately before transmission is multiplied by an integer between 1 and 35. Let the calculation result be 'x' ($0 \le x \le 2485$).

2a. For DC=1/3, one bit of real part of scrambling code is selected in the position which is at an x-chip apart from the boundary of gating group , as shown in FIG. 13A.. The selected one bit can be used for determining the position of gating slot in the following gating slot group. That is, the position of gating slot in current gating slot group can be determined based on the one bit selected in the previous gating slot group

2b. For DC=1/5, two bits of real part of scrambling code are selected in the position which is at an x-chip apart from the boundary of gating group, as shown in FIG. 13B.

3a. For DC=1/3, the position of a gating slot to be transmitted is determined using the selected one bit. Since only one bit is used, the position is randomly selected between two slots determined by the agreement, out of three transmittable slot positions.

3b. For DC=1/5, the position of a slot to be transmitted is determined using the selected two bits. Since the two bit are used, the positions are randomly selected among four slot positions determined by the agreement, out of five transmittable slot positions.

4. When the SFN is changed, the above procedure is performed again from step 1 with a new value. In this case, the integer value used in step 1 (ranges from 1 to 35) is maintained.

For the positions of the transmission gating slots of the downlink , the downlink gating pattern (or downlink gated transmission pattern) is equal to that of uplink. For efficient power control, however, a specific offset may exist between uplink and downlink gating-on slot. This offset is given as a system parameter. In addition, the downlink gating pattern can be determined using preset positions, regardless of the uplink gating pattern.

FIG. 14A shows a method for selecting gating positions of the gating slot groups for DC=1/3. The gating position controller 242 of the mobile station receives a scrambling code and SFN of the downlink signal, and selects one bit in the real part of the scrambling code. The selected one bit is utilized for determining the gating-on slot of the next gating slot group. In other words, the position of gating-on slot in current gating slot group is determined based on the one bit selected in the previous gating slot group. In general, the time difference in unit of slot between current gating slot group and the gating slot group from which the one bit is selected can be larger than one. Here, the base station transmits the downlink gating slot in the position which is a predetermined number of slots off from the position of the

gating slot received in the uplink.

FIG. 14B shows a method for selecting gating positions of the gating slot groups for DC=1/5. The gating position controller 242 of the mobile station receives a scrambling code and SFN of the downlink signal, and selects two bits in the real part of the scrambling code. The selected two bits are utilized for determining the gating-on slot of the next gating slot group. In other words, the position of gating-on slot in current gating slot group is determined based on the two bits selected in the previous gating slot group. In general, the time difference in unit of slot between current gating slot group and the gating slot group from which the two bits are selected can be larger than one. Here, the base station transmits the downlink gating-on slot in the position which is a predetermined number of slots off from the position of the gating-on slot received in the uplink.

When determining a location of real part of scrambling code, it is also possible to use the channelization code number for the downlink signal, which is uniquely applied to each mobile station, in addition to the SFN. Using the channelization code for the downlink signal is to prevent the downlink signals for the different mobile stations from transmitting the gating slots in the same time position.

Another method for selecting the gating slot in a gating slot group is shown in FIGs 13C, 13D, 14C, and 14D. In this method, the gating positions are determined by performing modulo-3 or modulo-5 operation on the decimal value of N bits from specific portion of real part of scrambling code.

A second method for randomly selecting an arbitrary slot in a gating slot group unit according to this embodiment of the present invention is determined in the following order.

1. A system frame number (SFN) 0 to 71 of a signal received immediately before transmission is multiplied by an integer between 1 and 35. Let the calculation result be 'x'($0 \le x \le 2485$).

2a. For DC=1/3, N bits of the real part of scrambling code are selected in the

position which is at an x-chip apart from the boundary of gating slot group, as shown in FIG 13C. The selected N bits can be used for determining the position of gating slot in the following gating slot group. That is, the position of gating slot in current gating slot group can be determined based on the N bits selected in the previous gating slot group.

2b. For DC=1/5, N bits of the real part of scrambling code are selected in the position which is at an x-chip apart from the boundary of gating slot group, as shown in FIG 13D. The selected N bits can be used for determining the position of gating slot in the following gating slot group. That is, the position of gating slot in current gating slot group can be determined based on the N bits selected in the previous gating slot group.

3a. For DC=1/3, the position of a gating slot to be transmitted is determined using a value obtained by performing a modulo-3 operation on a decimal value corresponding to the selected N bits. Since the resulting value of the modulo-3 operation is one of 0, 1 and 2, each value designates the position of an arbitrary slot in the gating duration (or gating slot group).

3b. For DC=1/5, the position of a slot to be transmitted is determined using a value obtained by performing a modulo-5 operation on a decimal value corresponding to the selected N bits. Since the resulting value of the modulo-5 operation is one of 0, 1, 2, 3 and 4, each value designates the position of an arbitrary slot in the gating gating slot group.

4. When the SFN is changed, the above procedure is performed again from step 1 with a new value of offset x. In this case, the integer value used in step 1 (ranges from 1 to 35) is maintained.

The gating slot position selecting method selects the gating position of the gating slot group using the real part of scrambling code and SFN which ranges from 0 to 71. Therefore, the gating-on slot pattern has a period of 720msec. In order to make the period of gating-on pattern greater than 720msec, the x value can be changed whenever the SFN becomes a specific value.

FIG. 14C shows a method for selecting gating positions of the gating slot

groups for DC=1/3. The gating position controller 242 of the mobile station receives a scrambling code and SFN of the downlink signal, selects N bits in the real part of the scrambling code. The selected one bit is utilized for determining the gating slot of the next gating slot group. In other words, the position of gating slot in current gating slot group is determined based on the modulo-3 operation of N bits selected in the previous gating slot group. In general, the time difference in unit of slot between current gating slot group and the gating slot group from which N bits are selected can be larger than one. Here, the base station transmits the downlink gating slot in the position that is a predetermined number of slots off from the position of the gating slot received in the uplink..

FIG. 14D shows a method for selecting gating positions of the gating slot group for DC=1/5. The gating position controller 242 of the mobile station receives a scrambling code and SFN of the downlink signal, and selects N bits in the real part of the scrambling code. The selected N bits are utilized for determining the gating slot of the next gating slot group. In other words, the position of gating slot in current gating slot group is determined based on the modulo-5 operation of N bits selected in the previous gating slot group. In general, the time difference in unit of slot between current gating slot group and the gating slot group from which N bits are selected can be larger than one. Here, the base station transmits the downlink gating slot in the position that is a predetermined number of slots off from the position of the gating slot received in the uplink.

Arranging the gating positions of the slots irregularly is to prevent electromagnetic wave-related bad effects due to the power of the regularly transmitted signals. In order to randomly gate the transmission signals, this embodiment gives an example of using an arbitrary number for distinguishing the uplink/downlink frame together with an uplink scrambling code or a fixed sequence. The arbitrary number for distinguishing the uplink/downlink frame can become SFN or CFN (Connection Frame Number), and can also become an arbitrary system parameter for determining the uplink/downlink frame. The second method for gating a randomized slot in a gating slot group according to this embodiment of the present invention randomly gates a randomized slot in the using the CFN. That is, the second random gating method according to this embodiment of the present invention uses the CFN as an arbitrary number for distinguishing the uplink/downlink frame, and the CFN is a value which is equally used by every base station in

communication with a specific mobile station (or user equipment). Further, the CFN is indicated by 8 bits and is a frame number having a repetition period of 256(0 to 255).

FIG. 15A shows a method for extracting a partial sequence required in generating a gating pattern from an uplink scrambling code. The scrambling code for the uplink signal is used for distinguishing the user equipment (UE) in the mobile communication system, and is classified into a long scrambling code and a short scrambling code. The long scrambling code has a length of 33,554,432 bits, and is applied to a one-frame signal transmitted from the user equipment using only a 38400-bit length code consisting of the 0^{th} to 38399^{th} bits of the full length, to distinguish the user equipment. The short scrambling code has a length of 256 bits and is repeated 150 times within one frame transmitted from the user equipment. The short scrambling code is a user identification scrambling code used for the case where the base station includes a separate device such as an interference remover.

Referring to FIG. 15A, a slot 1511 is a first slot of a frame 1501 and has a slot number 0. For a scrambling code applied to the slot 1511, the long scrambling code uses 0^{th} to 2559^{th} bits, and the short scrambling code repeats a scrambling code of 0^{th} to 255^{th} bits 10 times. In the following description, the long scrambling code and the short scrambling code will be both called a scrambling code. The long scrambling code and short scrambling code can be used in this invention. In FIG. 15A, reference numeral 1512 indicates a 0^{th} bit of the scrambling code of the first slot 1511, reference numeral 1513 indicates a 1^{st} bit of the scrambling code, and reference numeral 1514 indicates 2559^{th} bit of the scrambling code.

In FIG. 15A, reference numeral 1501 indicates 1-frame duration The frame 1501 is comprised of 15 slots from the 0^{th} slot 1511 to the 14^{th} slot 1519. A description of a method for selecting the gating slot position of the gating slot group in frame 1501 will be made below.

The frame 1501 is divided into gating slot groups each including 3 or 5 slots according to the DC. That is, for DC=1/3, the frame 1501 is divided into 5 gating slot groups each including 5 slots (i.e., gating slot group #0 includes 0^{th} to 2^{nd} slots, gating slot group #1 includes 3^{rd} to 5^{th} slots, gating slot group #2 includes 6^{th} to 8^{th} slots, gating slot group #3 includes 9^{th} to 11^{th}, and gating slot group #4 includes 12^{th}

to 14th slots). For DC=1/5, the frame 1501 is divided into 3 gating slot groups each including 5 slots (i.e., gating slot group #0 includes 0th to 4th slots, gating slot group #1 includes 5rd to 9th slots, gating slot group #2 includes 10th to 14th slots).

In FIG. 15A, the frame 1501 is divided into 3 or 5 gating slot groups according to the DC, and each gating slot group has an offset value that is equal to the gating slot group numbers for the respective gating slot groups. For DC=1/3, the offset values of gating slot group#0 is 0, the offset value of gating slot group#1 is 1, the offset value of gating slot group#2 is 2, the offset value of gating slot group#3 is 3, and the offset value of gating slot group#4 is 4. For DC=1/5, the offset value of gating slot group#0 is 0, the offset value of gating slot group#1 is 1, and the offset value of gating slot group#2 is 2. Application of the offset values will be described below.

1551st to 1554th bits of FIG. 15A indicate the n extracted bits. Therefore, the n bits of 1551st to 1554th bits are selected from the 0th bit 1512 to the 2559th bit 1514 of the scrambling code used for the slot 1511 according to the prescribed agreement between a base station and a mobile station. Here, 'n' is a multiple of 8, and is a positive number which can be arbitrarily set. A method for selecting the n bits from bit 1551 to bit 1554 in the scrambling code applied to the slot 1511 is as follows. In order to decide the gating slot in current gating slot group, n bits from the scrambling code used in the previous gating slot group with an offset is utilized, where the offset is applied to the first bit of the scrambling code of the previous gating slot group.

(1) For DC=1/3, the frame is divided into 5 gating slot groups #0 to #4. For the n bits used for selecting the gating position of the gating slot group #0, n bits starting from the 30724th bit of the scrambling code of the preceding frame are used.. Here, the 30724th bit is the bit to which offset of 4 is applied from the boundary of the gating slot group#4 of the previous frame. That is, it is the 30720th bit, which is the start bit of the scrambling code applied to the gating slot group #4 of the previous frame. And the start bit of the n bits(which will be used for the gating slot group #0 in current frame) is 30724th bit which is determined by applying an offset value of gating slot group #4(=4) of the previous frame of the gating slot group #0. Accordingly, the start bit for selecting a scrambling code used in selecting the gating position to be applied to the gating slot group #0 becomes the 30724th bit.

Similarly, for the n bits used for selecting the gating position in the gating slot group #1, n bits are sequentially extracted starting from the 0^{th} bit of the scrambling code of the gating slot group #0 because the offset value for the gating slot group#0 is 0. For the n bits used for selecting the gating position in the gating slot group #2, n bits are sequentially extracted starting from the 7681^{st} bit of the scrambling code by applying an offset value (i.e., offset value=1) of the gating slot group #1. For the n bits used for selecting the gating position in the gating slot group #3, n bits are sequentially extracted starting from the 15362^{nd} bit of the scrambling code by applying an offset value (i.e., offset value=2) of the gating slot group #2. For the n bits used for selecting the gating position in the gating slot group #4, n bits are sequentially extracted starting from the 23043^{rd} bit of the scrambling code by applying an offset value (i.e., offset value=3) of the gating slot group #3. As described previously, for the n bits used for selecting the gating position in the gating slot group #0, n bits are sequentially extracted starting from the 30724^{th} bit of the scrambling code by applying an offset value (i.e., offset value=4) of the gating slot group #4 of the previous frame. In other words, the n bits used to determine the gating slot position within gating slot group #(p+1) are selected starting from bit number y, where y= {1^{st} bit of gating slot group #(p)} + {the offset of gating slot group #(p)} except for determining the gating slot position within gating slot group#0. In case of the gating slot position within gating slot group#0, n bits used to determine the gating slot position within gating slot group#0 are selected starting from bit number y, where y={1^{st} bit of gating slot group#4 of the previous frame} + {the offset of gating slot group#4}.

In other words, the n bits used to determine the gating slot position within gating slot group #(p+1) are selected starting from bit number y, where y= {1^{st} bit of gating slot group #(p)} + {the offset of gating slot group #(p)} except for determining the gating slot position within gating slot group#0. In case of the gating slot position within gating slot group#0, n bits used to determine the gating slot position within gating slot group#0 are selected starting from bit number y, where y={1^{st} bit of gating slot group#4 of the previous frame} + {the offset of gating slot group#4}.

(2) For DC=1/5, the frame is divided into 3 gating slot groups of the gating slot groups #0 to #2. For the n bits used for selecting the gating position of within the gating slot group #0, n bits are sequentially extracted starting from the 25602^{nd}

bit of the scrambling code of the previous frame. For the n bits used for selecting the gating position of the gating slot group #1, n bits are sequentially extracted starting from the 0^{th} bit of the scrambling code. For the n bits used for selecting the gating position of the gating slot group #2, n bits are sequentially extracted starting from the 12801^{st} bit of the scrambling code.

FIG. 15B is a diagram for explaining a third method for performing random gating according to an embodiment of the present invention. This method is implemented using CFN. FIG. 15B shows a method for extracting an n-bit sequence required in generating a gating pattern from a fixed sequence A.

Referring to FIG. 15B, the n-bit(16 bit) sequences are used in determining the irregular transmission pattern in each gating slot group. The n-bit(16 bit) sequences are obtained by applying offset j(0, 1, 2, 3) shift selection from the fixed sequence (ie, A=a0, a1, a2 ... a18=1011010011011101001). For DC 1/5, A_0 and A_1 can be used. The A_0 have 16 bits(a0 to a15) and A_1 have 16 bits(a1 to a16). For DC 1/3, A_0, A_1, A_2 and A_3 can be used. At that case, the A_0 is a0 to a15 extracted from the fixed sequence A with offset 0, the A_1 is a1 to a16 extracted from the fixed sequence A with offset 1, the A_2 is a2 to a17 extracted from the fixed sequence A with offset 2, and the A_3 is a3 to a18 extracted from the fixed sequence A with offset 3. The A_0 will be used for calculating the gating slot of the 0'th gating slot group and the A_1 will be used for calculating the gating slot of the 1'th gating slot group. The A_2 and A_3 will be used for calculating the gating slot of the 2'th and 3'th gating slot group when the DC is 1/3. Therefore, the A_0 and A_1 or A_0 to A_3 is periodically used in each frame. In FIG. 15B, the n-bit sequence is shown which is obtained by applying the offset to the fixed sequence A where the value of offset is equal to the current gating slot group number. Since the sequence to be used in each gating slot group is selected by applying an offset to the fixed sequence A, the following sequences cannot be used A.

1. The case where the sequences selected after applying the offset become equal.

Ex) A=10101010101010101010
Offset 0 : A_0=10101010101010101010
Offset 1 : A_1=01010101010101010101
Offset 2 : A_2=10101010101010101010

2. Sequence of all 1's or all 0's
Ex) A=00000000000000000000000
Ex) A=11111111111111111111

An exemplary hardware structure for selecting the gating position using the n bits used in selecting the gating slot position of FIGS. 15A and 15B is shown in FIG. 16. FIG. 16 shows an apparatus to perform a method for selecting the gating slot position by using the uplink scrambling code shown in FIG. 15A together with CFN, or the fixed sequence A shown in FIG. 15B together with the CFN.

Referring to FIG. 16, a memory 1601 stores the n bits of the scrambling code selected in the manner described with reference to FIG. 15A or stores the n bits(ie, 16bit) from the fixed sequence Aaccording to the selecting manner described with reference to FIG. 15B.

A memory 1603 stores the repeated CFN, by the n-bit(16 bits) length, which is equally used in the user equipment and a base station in communication with the user equipment. The CFN is repeatly increased 0 to 255 which can be represented by 8 bits, and is stored in the memory 1603, after being repeated n/8 times in order that the length of bits stored in memory 1603 equal the value of 'n'. A bit 1631 stored in the memory 1603 is the 0^{th} bit which is the most significant bit (MSB) of the CFN, and a bit 1638 is the 7^{th} bit which is the least significant bit (LSB) of the CNF. A bit 1639 stored in the memory 1603 is the MSB of the CFN and has the same value as the bit 1631, and a bit 163n is the LSB of the CFN and has the same value as the bit 1638. In the memory 1603 of FIG. 16, the order of the MSB and the LSB of the CFN can be changed.

A multiplier 1604 of FIG. 16 is comprised of n exclusive OR (XOR) operators 1641-164n. The multiplier 1604 performs an XOR operation on the n bits stored in the memory 1601 and the CFN bits stored in the memory 1603, and provides the operation results to a decimal converter 1605. That is, the n XOR operators 1641-164n XOR the bits 1611-161n output from the memory 1601 and the bits 1631-163n output from the memory 1603.

The decimal converter 1605 converts the operation results of the multiplier

1604 to a decimal number. That is, the decimal converter 1605 includes memories 1651-165n for storing n operation values output from the XOR operators 1641-164n of the multiplier 1604, and converts the operation values stored therein to a decimal number. A value of the decimal number is determined according to the value of 'n'. The decimal number output from the decimal converter 1605 is provided to a modulo operator 1607. The modulo operator 1607 outputs a value which depends on the DC value. For DC=1/3, the modulo operator 1607 outputs one of 0, 1 and 2. For DC=1/5, the modulo operator 1607 outputs one of 0, 1, 2, 3 and 4. The slots not to be transmitted in the gating slot group to which the output results of the modulo operator 1607 are applied, are determined based on the output results. The decimal converter 1605 and the modulo operator 1607 can also be implemented by software.

The descriptions of FIG. 15A and 16 can be expressed by Equation (1) below.

$$N(G,C^i)=\left(\sum_{l=0}^{15}\left(S\left(G_{prev}\times 2560\times\frac{1}{T}+G_{prev}+l\right)\oplus C^i_{(k \bmod 8)}\right)\times 2^{15-l}\right)\bmod T \quad (1)$$

where, G : current gating slot group number,

G_{prev} : previous gating slot group number,

C^i : CFN number of ith frame $(=(C^i_0C^i_1C^i_2C^i_3C^i_4C^i_5C^i_6C^i_7)_2)$, and

T : the reciprocal of the DC.

S: Scrambling code

For a better understanding of Equation (1), a description will be made of FIGS. 15A and 16 for the case where the present gating slot group is 1, n=16 , CFN= 10001100_2, and DC=1/3.

The 16-bit value '1101001010111000' of the scrambling code selected in the manner of FIG. 15A is stored in the memory 1601 of FIG. 16. Further, since CNF= 10001100, a value '1000110010001100' is stored in the memory 1603 of FIG. 16. The multiplier 1604 is comprised of 16 XOR operators, and outputs an XOR operation value '0101111000110100'. The decimal converter 1605 converts the

output value of the multiplier 1604 to a decimal value '11,386'(or '24,116'). For DC=3, the modulo operator 1607 performs a modulo-3 operation on the output value '11,386' (or '24,116') of the decimal converter 1605 and outputs a value 1 (or 2 in case of '24,116'). Therefore, out of 3 slots in the gating slot group #2, a second (or third) slot is transmitted for transmitting TFCI, TPC and pilot symbol which are control data on the DPDCH.

The descriptions of FIG. 15B and 16 can be expressed by Equation (2) below.

$$s(i,j)=\begin{cases}(A_j \oplus C_i)\bmod(S_G-1)+1, & j=0 \\ (A_j \oplus C_i)\bmod S_G, & j=1,2,...,N_G-2, \\ S_G-1, & j=N_G-1\end{cases} \qquad i=0,1,...,255 \quad ....(2)$$

where, A_j : a sequence obtained by applying j bit offset to the fixed sequence A,
C_i : a sequence obtained by repeating current CFN,
S_G : the number of slots constituting one gating slot group, and
N_G : the number of gating slot groups constituting one frame.

A detailed description of Equation (2) will be made below.

In Equation (2), s(i,j) indicates a slot number, which should be transmitted, out of the slots constituting a jth gating slot group of an ith frame. Here, the slot number is not assigned in a frame unit, but assigned in a gating slot group unit. A_j indicates the n bit sequence obtained by applying a j offset to the fixed sequence A as shown in FIG 15B, where the amount of offset j is equal to each gating slot group number.C_i indicates an n-bit sequence created by repeating the current CFN (8 bits). The CFN is a connection frame number. The base station and the mobile station repeatedly count the CFN(0 to 255) starting at the beginning of the connection. S_G indicates the number of slots in one gating slot group. For DC=1/3, S_G is 3 and for DC=1/5, S_G is 5. N_G indicates the number of gating slot groups in one frame. For DC=1/3, N_G is 5, and for DC=1/5, N_G is 3. For j=0 (i.e., in the first gating slot group of the frame) A_0 and current CFN(C_i) are XORed and then '1' is added to a value

obtained by performing a modulo(S_G-1) operation on the XORed value. As the result of this operation, the first slot of every frame is always gated off (i.e., not transmitted). Further, for j=N_G-1 (i.e., in the last gating slot group of the frame), only the last slot S_G-1 is always gated on (i.e., transmitted). For the other gating slot groups (0<j<N_G-1), A_j and C_i are XORed and then a modulo-S_G operation is performed on the XORed value. The reason for processing the first and last gating slot groups differently from the other gating slot groups is to assist in channel estimation. FIG 15C shows the generation rule. It is also possible to determine the gating position using Equation (3) below in which the same rule is applied to every .

$$s(i,j) = (A_j \oplus C_i) \bmod S_G, \qquad j = 0,1,2,..,,,.N_G - 1, \qquad i = 0,1,...,255 .. . \quad (3)$$

An operation of determining the gating position of the slots in the gating slot group using Equations (2) and (3) will be described with reference to FIGS. 16, 10A and 10B.

The structure of FIG. 16 corresponds to the gating position selector 150 of FIG. 10A and the gating position selector 250 of FIG. 10B. An operation of the gating position selector will be described with reference to FIG. 16.

The memory 1601 stores the n bits selected in the manner described with reference to FIG. 15B, and 'n' is a multiple of 8, which is a positive number. Here, the sequence stored in the memory 1601 is a sequence A_j obtained by applying j bit offset to the fixed sequence A. A memory 1603 stores the repeated CFN, of n-bit length, which is equally used in the user equipment and every base station in communication with the user equipment. A sequence stored in the memory 1603 is a sequence C_i obtained by repeating the current CFN. The multiplier 1604 comprised of n XOR operators, performs an XOR operation on the sequence A_j and the sequence C_i stored in the memories 1601 and 1603 in a bit unit to generate the operation result of $A_j \oplus C_i$, and provides the operation result to the decimal converter 1605. The decimal converter 1605 converts the operation result of the multiplier 1604 to a decimal number, and provides the converted decimal value to the modulo operator 1607. The modulo operator 1607 outputs a value which depends on the number, S_G, of the slots constituting one gating slot group. That is, when S_G is 3 (i.e.,

DC=1/5), the modulo operator 1607 outputs 0, 1 and 2, and when S_G is 5 (i.e., DC=1/3), the modulo operator 1607 outputs 0, 1, 2, 3 and 4.

In addition, the modulo operator 1607 can perform the same modulo operation as shown in Equation (2) according to the gating slot group number in one frame. That is, if the present gating slot group has the first gating slot group number in the frame, the gating position is determined such that the first slot data in the first gating slot group should not be transmitted. Otherwise, if the present gating slot group has the last gating slot group number, the gating position is determined such that the last slot data in the last gating slot group should be always transmitted.

The determined gating position information of each gating slot group is provided to the gated transmission controller 141 of FIG. 10A or the gated transmission controller 241 of FIG. 10B. The gated transmission controller gates on the data on the DPCCH in the slot duration of the gating position determined by the gating position selector, and gates off the data on the DPCCH in the other slot duration.

In order for the base station and the mobile station to perform gated transmission, the mobile communication system has the following state transition methods, which are determined according to system setup. In one method, transition occurs by a set timer value or a transition command message from the base station. In another method, transition occurs sequentially while changing the gating rate. At this point, the gating rate DC can be determined in consideration of a capacity of the corresponding mobile station and the channel environments. Assume that one frame is comprised of 16 slots. Then, in the former transition method, a direct gating rate transition occurs from DC=1/1 to DC=1/2, from DC=1/1 to DC=1/4, or from DC=1/1 to DC=1/8. In the latter transition method, a sequential gating rate transition occurs from DC=1/1 to DC=1/2, from DC=1/2 to DC=1/4, and from DC=1/4 to 1/8. The gated transmission method according to an embodiment of the present invention will be described for both the case where one frame is comprised of 16 slots and the case where one frame is comprised of 15 slots. When one frame is comprised of 16 slots, the gating rate can become 1/2, 1/4 and 1/8, and when one frame is comprised of 15 slots, the gating rate can become 1/3 and 1/5.

FIGS. 7A and 7B show the uplink DPCCH for the case where a dedicated

MAC (Medium Access Control) logical channel is generated and a corresponding transition message is transmitted over the uplink DPDCH when there is no DPDCH data for a predetermined period of time of FIGS. 6A and 6B.

Reference numeral 311 of FIG. 7A shows a case where an uplink DPDCH message is generated while the uplink DPCCH does not undergo gated transmission (i.e., while the uplink DPCCH is continuously transmitted (DC=1/1)). Reference numeral 312 shows a case where the uplink DPDCH message is generated while the uplink DPCCH undergoes DC=1/2 gated transmission. Reference numeral 313 shows a case where the uplink DPDCH message is generated while the uplink DPCCH undergoes DC=1/4 gated transmission. Reference numeral 314 shows a case where the uplink DPDCH message is generated while the uplink DPCCH undergoes DC=1/8 gated transmission. Even for slots, which are not transmitted in the gated transmission pattern as shown by the reference numerals 312, 313 and 314, the slots in the corresponding duration undergo normal transmission when the uplink DPDCH is transmitted in the corresponding duration. In the slots for normal transmission, the TPC bits for downlink power control can be omitted and the pilot duration (or period) can be extended to a slot length before transmission. Beginning at the slots succeeding after transmitting the uplink DPDCH message by normal transmission of the slots, it is possible to transmit the uplink DPCCH without gating, or it is possible to continue the gated transmission at the original gating rate until a gating stop message is received from the base station. That is, when the uplink DPDCH message is transmitted during DC=1/2 gated transmission, it is possible to perform normal transmission on the slot of the above duration, thereafter perform DC=1/2 gated transmission again, and then stop gated transmission (DC=1) when transmitting user data after receiving a gating stop message from the base station.

As in the case of the uplink DPCCH, even for the slots which are not transmitted in the gated transmission pattern, the slots undergo normal transmission in the corresponding duration, when a downlink DPDCH message is generated during gated transmission for the downlink DPCCH. In the slots for normal transmission, the TPC bits for uplink power control can be omitted and the pilot duration can be extended to a slot length. Beginning at the slots succeeding after transmitting the downlink DPDCH message by normal transmission of the slots, it is possible to transmit the downlink DPCCH without gating, or it is possible to continue the gated transmission at the original gating rate until a gating stop request

message is received from the mobile station. That is, when the downlink DPDCH message is transmitted during DC=1/2 gated transmission, it is possible to perform normal transmission on the slot of the above duration, thereafter perform DC=1/2 gated transmission again, and then stop gated transmission (DC=1) when transmitting the user data after receiving a gating stop request message from the mobile station.

Reference numeral 315 of FIG. 7B shows a case where an uplink DPDCH message is generated while the uplink DPCCH undergoes DC=1/2 gated transmission. Reference numeral 316 shows a case where the uplink DPDCH message is generated while the uplink DPCCH undergoes DC=1/4 gated transmission. Reference numeral 317 shows a case where the uplink DPDCH message is generated while the uplink DPCCH undergoes DC=1/8 gated transmission. Even for the slots, which are not transmitted in the gated transmission pattern as shown by the reference numerals 315, 316 and 317, the slots in the corresponding duration undergo normal transmission when the uplink DPDCH is transmitted in the corresponding duration. In the slots for normal transmission, the TPC bits for downlink power control can be omitted and the pilot duration can be extended to a slot length before transmission. Beginning at the slots succeeding after transmitting the uplink DPDCH message by normal transmission of the slots, it is possible to transmit the uplink DPCCH without gating, or it is possible to continue the gated transmission at the original gating rate until a gating stop message is received from the base station. That is, when the uplink DPDCH message is transmitted during DC=1/2 gated transmission, it is possible to perform normal transmission on the slot of the above duration, thereafter perform DC=1/2 gated transmission again, and then stop gated transmission (DC=1) when transmitting user data after receiving a gating stop message from the base station.

It is also possible to simultaneously gate transmission of both the uplink DPCCH and the downlink DPCCH in the same gating pattern. Beginning at the slots succeeding after transmitting the downlink DPDCH message by normal transmission of the slots, generated while gating transmission of the downlink DPCCH, it is possible to transmit the downlink DPCCH without gating, or it is possible to gate transmission of the downlink DPCCH at the original gating rate until a gating stop message is received from the mobile station. That is, when the downlink DPDCH message is transmitted during DC=1/2 gated transmission, it is

possible to perform normal transmission on the slot of the above duration, thereafter perform DC=1/2 gated transmission again, and then stop gated transmission (DC=1) when transmitting the user data after receiving a gating stop message from the mobile station.

FIG. 8A shows a method for transmitting downlink and uplink signals when transmission of a downlink DPDCH is discontinued. When transmission of the downlink DPDCH is discontinued as shown by reference numeral 801 in the RBA mode where the uplink DPDCH has no traffic data to transmit, the base station and the mobile station start gating if a set timer value expires and a gating start message is received. Although FIG. 8A shows an embodiment where the gating start message is generated by the base station, it is also possible for the mobile station to send a gating-request message to the base station when there is no downlink and uplink DPDCH. While transmitting the downlink DPCCH in FIG. 8A, it is also possible to transmit all the TFCI, TPC and pilot symbols without gating. Since the TPC bits include meaningless TPC values determined by measuring power strength of the pilot symbols of the gated slots within the uplink DPCCH, the mobile station ignores the meaningless TPC values transmitted from the base station in order to perform uplink power control in consideration of the gating pattern for the uplink DPCCH, and performs transmission at the same transmission power as the transmission power for the previous slot.

Alternatively, while transmitting the downlink DPCCH in FIG. 8A, it is also possible to gate only the TFCI and TPC bits in the downlink DPCCH without gating the pilot symbols in the downlink DPCCH. At this point, the gating pattern is identical to a gating pattern for the uplink DPCCH of the mobile station. The slot, in which the TPC bits in the downlink DPCCH are gated, refers to the TPC bits generated by measuring the pilot symbols corresponding to the gated slot in the DPCCH transmitted from the mobile station.

Reference numeral 802 shows a situation where a message generated by the base station is transmitted to the mobile station over the downlink DPDCH. In this case, the mobile station, which has been gating transmission of the uplink DPCCH, can stop gated transmission and perform normal transmission (DC=1) after receiving the message. Alternatively, the mobile station, which has been gating transmission of the uplink DPCCH, can continue gated transmission even after receiving the

message, and then perform normal transmission (DC=1) upon receipt of a gating stop message.

FIG. 8B shows a method for transmitting downlink and uplink signals when transmission of an uplink DPDCH is discontinued. When transmission of the downlink DPDCH is discontinued as shown by reference numeral 803 in the RBA mode where there exists no downlink DPDCH, the base station and the mobile station make a state transition at a time point appointed (or scheduled) between them when a set timer value expires or after exchanging a state transition message. Although FIG. 8B shows an embodiment where the state transition message is generated through the downlink DPDCH, the state transition message can be generated even in the uplink DPDCH of the mobile station. While transmitting the downlink DPCCH of FIG. 8B, it is possible to transmit all the TFCI, TPC and pilot symbols without gating. Since the TPC bits include meaningless TPC values determined by measuring power strength of the pilot symbols of the gated slots within the uplink DPCCH, the mobile station ignores the meaningless TPC values transmitted from the base station in order to perform uplink power control in consideration of the gating pattern for the uplink DPCCH, and performs transmission at the same transmission power as the transmission power for the previous slot.

Alternatively, while transmitting the downlink DPCCH in FIG. 8B, it is also possible to gate only the TFCI and TPC bits in the downlink DPCCH without gating the pilot symbols in the downlink DPCCH. At this point, the gating pattern is identical to a gating pattern for the uplink DPCCH of the mobile station. The slot, in which the TPC bits in the downlink DPCCH are gated, refers to the TPC bits generated by measuring the pilot symbols corresponding to the gated slot in the DPCCH transmitted from the mobile station.

Reference numeral 804 shows a situation where a state transmission message generated by the base station is transmitted to the mobile station over the downlink DPDCH. In this case, the mobile station, which has been gating transmission of the uplink DPCCH, can stop gated transmission and perform normal transmission (DC=1) upon receipt of the state transition message. Alternatively, the mobile station, which has been gating transmission of the uplink DPCCH, can continue gated transmission even after receipt of the state transition message, and

then stop gated transmission and perform normal transmission (DC=1) at a state transition point designated by the state transition message.

FIG. 8C shows a method for transmitting downlink and uplink signals when transmission of a downlink DPDCH is discontinued. When transmission of the downlink DPDCH is discontinued as shown by reference numeral 805 in the RBA mode where there exists no uplink DPDCH, the base station and the mobile station transition to the RBS mode if a set timer value expires or a downlink DPDCH message for state transition is generated. Although FIG. 8C shows an embodiment where the message for state transition to the RBA mode is generated by the base station, it is also possible for the mobile station to send a state transition request message to the base station when there is no downlink and uplink DPDCH. While transmitting the downlink DPCCH in FIG. 8C, it is also possible to transmit all the TFCI, TPC and pilot symbols without gating. Since the TPC bits include meaningless TPC values determined by measuring the power strength of the pilot symbols of the gated slots within the uplink DPCCH, the mobile station ignores the meaningless TPC values transmitted from the base station in order to perform uplink power control in consideration of the gating pattern for the uplink DPCCH, and performs transmission at the same transmission power as the transmission power for the previous slot.

Alternatively, while transmitting the downlink DPCCH in FIG. 8C, it is also possible to gate only the TFCI and TPC bits in the downlink DPCCH without gating the pilot symbols in the downlink DPCCH. At this point, the gating pattern is identical to a gating pattern for the uplink DPCCH of the mobile station. The slot, in which the TPC bits in the downlink DPCCH are gated, refers to the TPC bits generated by measuring the pilot symbols corresponding to the gated slot in the DPCCH transmitted from the mobile station.

Reference numeral 806 shows a situation where a state transition message generated by the mobile station is transmitted to the base station over the uplink DPDCH. In this case, the mobile station, which has been gating transmission of the uplink DPCCH, can stop gated transmission and then perform normal transmission (DC=1) after transmission of the state transition message over the uplink DPDCH. Alternatively, the mobile station, which has been gating transmission of the uplink DPCCH, can continue gated transmission even after transmission of the state

transition message, and then stop gated transmission and perform normal transmission (DC=1) at the state transition point.

FIG. 8D shows a method for transmitting downlink and uplink signals when transmission of an uplink DPDCH is discontinued. When transmission of the uplink DPDCH is discontinued as shown by reference numeral 807 in the RBA mode where there exists no downlink DPDCH, the base station and the mobile station make a state transition at a time point appointed between them when a set timer value expires or after exchanging a state transition message. Although FIG. 8D shows an embodiment where the state transition message is generated through the downlink DPDCH, the state transition message can also be generated in the uplink DPDCH of the mobile station. While transmitting the downlink DPCCH in FIG. 8D, it is also possible to transmit all the TFCI, TPC and pilot symbols without gating. Since the TPC bits include meaningless TPC values determined by measuring power strength of the pilot symbols of the gated slots within the uplink DPCCH, the mobile station ignores the meaningless TPC values transmitted from the base station in order to perform uplink power control in consideration of the gating pattern for the uplink DPCCH, and performs transmission at the same transmission power as the transmission power for the previous slot.

Alternatively, while transmitting the downlink DPCCH in FIG. 8D, it is also possible to gate only the TFCI and TPC bits in the downlink DPCCH without gating the pilot symbols in the downlink DPCCH. At this point, the gating pattern is identical to a gating pattern for the uplink DPCCH of the mobile station. The slot, in which the TPC bits in the downlink DPCCH are gated, refers to the TPC bits generated by measuring the pilot symbols corresponding to the gated slot in the DPCCH transmitted from the mobile station.

Reference numeral 808 shows a situation where a state transition message generated by the mobile station is transmitted to the base station over the uplink DPDCH. In this case, the mobile station, which has been gating transmission of the uplink DPCCH, can stop gated transmission and then perform normal transmission (DC=1) after transmission of the state transition message over the uplink DPDCH. Alternatively, the mobile station, which has been gating transmission of the uplink DPCCH, can continue gated transmission even after transmission of the state transition message, and then stop gated transmission and perform normal

transmission (DC=1) at the state transition point.

FIG. 9A shows a method for transmitting downlink and uplink signals when transmission of a downlink DPDCH is discontinued. When transmission of the downlink DPDCH is discontinued, the base station and the mobile station make a state transition at a time point appointed between them if a set timer value expires or after exchanging a state transition message. FIG. 9A shows a case where the downlink DPCCH is gated in the same gating pattern as that of the uplink DPCCH. Although FIG. 9A shows an embodiment where the state transition message is transmitted through the downlink DPDCH, the state transition message can also be transmitted through the uplink DPDCH of the mobile station

FIG. 9B shows a method for transmitting downlink and uplink signals when transmission of an uplink DPDCH is discontinued. When transmission of the uplink DPDCH is discontinued, the base station and the mobile station make a state transition at a time point appointed between them if a set timer value expires or after exchanging a state transition message. FIG. 9B shows a case where a gating pattern for the downlink DPCCH is gated in the same gating pattern as that of the uplink DPCCH. Although FIG. 9B shows an embodiment where the state transition message is transmitted through the downlink DPDCH, the state transition message can also be transmitted through the uplink DPDCH of the mobile station.

In the foregoing drawings and descriptions, the downlink and uplink frames have the same frame starting point. However, in the UTRA (UMTS (Universal Mobile Telecommunications System) Terrestrial Radio Access) system, the starting point of the uplink frame is artificially delayed by 250μsec as compared with the starting point of the downlink frame. This is to make power control time delay become one slot (=0.625ms) in consideration of the propagation delay of the transmission signal when the cell radius is below 30km. Therefore, with due consideration of the artificial time delay between the downlink and uplink frame start time, the methods for gating transmission of the DPCCH signal are shown by FIGS. 11A to 11E. FIGS. 10A and 10B show structures of the base station transmitter and the mobile station transmitter, respectively, which enable such gated transmission.

FIG. 10A shows a structure of the base station transmitter according to

another embodiment of the present invention. The base station transmitter is different from FIG. 5A in that the pilot, TFCI and TPC bits constituting the downlink DPCCH can be separately gated in different gating patterns by the gated transmission controller 141. That is, the gated transmission controller 141 performs gated transmission on the pilot, TFCI and TPC bits for the downlink DPCCH at a slot (or time slot) scheduled with the mobile station in the RBS mode where the traffic data is not transmitted over the downlink and uplink DPDCHs. By using the gated transmission controller 141, it is also possible to assemble a pilot of an (n-1)th slot and TFCI and TPC bits of a nth slot in a gated transmission unit. When the base station transmits signaling data using the gated transmission controller 141 during gated transmission in the RBS mode, it is possible to avoid performing gated transmission on the pilot and TFCI in the duration where the signaling data is transmitted.

Alternatively, the gated transmission controller 141 can perform gated transmission on one slot (or one entire slot) including the pilot symbols, TFCI and TPC bits for the downlink DPCCH at a slot(or time slot) scheduled with the mobile station in the RBS mode where the traffic data is not transmitted over the downlink and uplink DPDCHs.

Although the downlink gating pattern is identical to the uplink gating pattern, there can exist an offset between them for efficient power control. The offset is given as a system parameter.

The gated transmission controller 141 can select the gating position of the slots either randomly or regularly according to the output of the gating position selector 250. That is, the gating position selector 250 can regularly determine the gating position of the slots. For example, for DC=1/3, 3rd, 6th, 9th, . . . slots are transmitted (or gated on). Further, the gating position selector 250 can randomly select the gating position of the slots in the method described with reference to FIGS. 15A, 15B and 16. In this case, the positions of the slots to be gated are determined by the random pattern.

FIG. 10B shows a structure of the mobile station transmitter according to another embodiment of the present invention. The mobile station transmitter is different from FIG. 5B in that the pilot, TFCI, FBI and TPC bits constituting the

uplink DPCCH can be separately gated in the different patterns by the gated transmission controller 241. The gated transmission controller 241 gates transmission of the pilot, TFCI, FBI and TPC bits for the uplink DPCCH at a power control group (or time slot) scheduled with the mobile station in the RBS mode where the traffic data is not transmitted over the downlink and uplink DPDCHs. When the base station transmits signaling data using the gated transmission controller 241 during gated transmission in the RBS mode, it is possible to avoid performing gated transmission on the pilot and TFCI in the duration where the signaling data is transmitted.

Alternatively, the gated transmission controller 241 can perform gated transmission on one slot including the pilot symbols, TFCI, FBI and TPC bits for the uplink DPCCH at a slot scheduled with the mobile station in the RBS mode where the traffic data is not transmitted over the downlink and uplink DPDCHs.

Although the downlink gating pattern is identical to the uplink gating pattern, there can exist an offset between them for efficient power control. The offset is given as a system parameter.

The gated transmission controller 141 can select the gating position of the slots either randomly or regularly according to the output of the gating position selector 250. That is, the gating position selector 250 can regularly determine the gating position of the slots. For example, for DC=1/3, 3^{rd}, 6^{th}, 9^{th}, . . . slots are transmitted (or gated on). Further, the gating position selector 250 can randomly select the gating position of the slots in the method described with reference to FIGS. 15A, 15B and 16. In this case, the positions of the slots to be gated are determined by the random pattern.

FIGS. 11A to 11D and FIGS. 12A to 12E show signal transmission diagrams for gated transmission performed by the base station and the mobile station transmitters of FIGS. 10A and 10B. FIGS. 11A to 11D show how to perform gated transmission when the frame length is 10msec and each frame includes 16 slots, i.e., each slot has a length of 0.625msec. FIGS. 12A to 12E show how to perform gated transmission when the frame length is 10msec and each frame includes 15 slots, i.e., each slot has a length of 0.667msec.

FIG. 11A shows gated transmission for the downlink and uplink DPCCHs according to a first embodiment of the present invention. As shown in FIG. 11A, a gated transmission unit for the downlink DPCCH may not be a slot unit. That is, in two adjacent slots, a pilot symbol of an nth slot and TFCI and TPC bits of an (n+1)th slot are set as a gated transmission unit for the downlink DPCCH. For example, when the gating rate is 1/2, a pilot symbol of slot number 0 and TFCI and TPC bits of slot number 1 are set as a gated transmission unit for the downlink DPCCH. When the gating rate is 1/4, a pilot symbol of slot number 2 and TFCI and TPC bits of slot number 3 are set as a gated transmission unit for the downlink DPCCH. When the gating rate is 1/8, a pilot symbol of slot number 6 and TFCI and TPC bits of slot number 7 are set as a gated transmission unit for the downlink DPCCH. Here, the gated transmission unit for the downlink DPCCH is set to be different from the actual slot unit, since an nth pilot symbol may be required in the receiver to demodulate the (n+1)th TPC according to a demodulation method for the TPC signal.

When a signaling message is generated during such gated transmission, the signaling message is transmitted over the downlink or uplink DPDCH. Therefore, performance of the frame starting point is very important. In the invention, as shown in FIG. 11A, the TPC for the downlink DPCCH and the TPC for the uplink DPCCH are located at slot number 15 (i.e., the 16^{th} slot, which is the last slot of the nth frame), so that the first slot of the (n+1)th frame is power controlled using the TPC bits existing in the last slot of an nth frame. That is, the TPC for power controlling the first slot of the next frame is located at the last slot of the present frame.

Meanwhile, in the UTRA system stated above, an offset between the downlink and uplink frame start points is fixed to 250μsec. However, for gated transmission of the downlink and uplink DPCCHs, the offset value can be changed to an arbitrary value while the base station and the mobile station exchange a parameter for DPCCH gated transmission in the call setup process. The offset value is set to a proper value in consideration of propagation delay of the base station and the mobile station in the call setup process. That is, when the cell radius is over 30Km, the offset value can be set to a value larger than the conventional offset value of 250μsec for DPCCH gated transmission, and this value can be determined through experiments.

FIG. 11B shows gated transmission for the downlink and uplink DPCCHs according to a second embodiment of the present invention. FIG. 11B shows a case where transmission of the downlink DPCCH goes ahead of transmission of the uplink DPCCH during gated transmission, for the gating rates of 1/2, 1/4 and 1/8. This difference (i.e., offset) is designated by "DL-UL timing" for the gating rates of 1/2, 1/4 and 1/8.

Referring to FIG. 11B, in two adjacent slots, a pilot symbol of an nth slot and TFCI and TPC of the (n+1)th slot are set as a gated transmission unit for the downlink DPCCH. For example, for the gating rate 1/2, a pilot symbol of slot number 0 and TFCI and TPC of slot number 1 are set as a gated transmission unit for the downlink DPCCH. For the gating rate 1/4, a pilot symbol of slot number 2 and TFCI and TPC of slot number 3 are set as a gated transmission unit for the downlink DPCCH. For the gating rate 1/8, a pilot symbol of slot number 6 and TFCI and TPC of slot number 7 are set as a gated transmission unit for the downlink DPCCH.

In addition, it is noted that the TPC for power controlling the first slot of the next frame is located at the last slot of the present frame. That is, the TPC for the downlink DPCCH and the TPC for the uplink DPCCH are both located at slot number 15 (i.e., the 16^{th} slot).

FIG. 11C shows gated transmission for the downlink and uplink DPCCHs according to a third embodiment of the present invention. FIG. 11C shows a case where transmission of the uplink DPCCH goes ahead of transmission of the downlink DPCCH during gated transmission, for the gating rates of 1/2, 1/4 and 1/8.

Referring to FIG. 11C, in two adjacent slots, a pilot symbol of a predetermined nth slot and TFCI and TPC of the (n+1)th slot are set as a gated transmission unit for the downlink DPCCH. For example, for the gating rate 1/2, a pilot symbol of slot number 1 and TFCI and TPC of slot number 2 are set as a gated transmission unit for the downlink DPCCH. For the gating rate 1/4, a pilot symbol of slot number 2 and TFCI and TPC of slot number 3 are set as a gated transmission unit for the downlink DPCCH. For the gating rate 1/8, a pilot symbol of slot number 6 and TFCI and TPC of slot number 7 are set as a gated transmission unit for the downlink DPCCH.

In addition, it is noted that the TPC for power controlling the first slot of the next frame is located at the last slot of the present frame. That is, the TPC for the downlink DPCCH and the TPC for the uplink DPCCH are both located at a slot number 15 (i.e., the 16^{th} slot).

FIG. 11D shows gated transmission for the downlink and uplink DPCCHs according to a fourth embodiment of the present invention. FIG. 11D shows a case where for the gating rates of 1/2, 1/4 and 1/8, transmission of the downlink DPCCH goes ahead of transmission of the uplink DPCCH during gated transmission, and the downlink and uplink gating patterns are set to the same period.

Referring to FIG. 11D, in two adjacent slots, a pilot symbol of the predetermined nth slot and TFCI and TPC of the (n+1)th slot are set as a gated transmission unit for the downlink DPCCH. For example, for the gating rate 1/2, a pilot symbol of slot number 0 and TFCI and TPC of slot number 1 are set as a gated transmission unit for the downlink DPCCH. For the gating rate 1/4, a pilot symbol of slot number 0 and TFCI and TPC of slot number 1 are set as a gated transmission unit for the downlink DPCCH. For the gating rate 1/8, a pilot symbol of slot number 2 and TFCI and TPC of slot number 3 are set as a gated transmission unit for the downlink DPCCH.

In addition, it is noted that the TPC for power controlling the first slot of the next frame is located at the last slot of the present frame. That is, the TPC for the downlink DPCCH and the TPC for the uplink DPCCH are both located at slot number 15 (i.e., the 16^{th} slot).

FIGS. 12A and 12B show gated transmission for the downlink and uplink DPCCHs according to a fifth embodiment of the present invention. FIGS. 12A and 12B show a case where a gating rate for gated transmission of the downlink and uplink DPCCHs is 1/3, i.e., gated on transmission is performed at the periods corresponding to 1/3 of the whole slots. That is, gated transmission is performed at the periods corresponding to 5 slots out of the whole 15 slots. At this point, a gated transmission unit for the downlink DPCCH is set to be different from a slot unit. That is, in two adjacent slots, a pilot symbol of the predetermined nth slot and TFCI and TPC of the (n+1)th slot are set as a gated transmission unit for the downlink

DPCCH. Accordingly, transmission is performed in the order of the pilot symbol of the nth slot and TPC and TFCI symbols of the (n+1)th slot.

In FIG. 12A, <Case 1> shows a case where the uplink DPCCH and the downlink DPCCH are simultaneously transmitted at the start of gated transmission, and the downlink and uplink gating patterns are set to the same period. With regard to two adjacent slots, a pilot symbol of slot number 1 and TFCI and TPC of slot number 2 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 4 and TFCI and TPC of slot number 5 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 7 and TFCI and TPC of slot number 8 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 10 and TFCI and TPC of slot number 11 are set as a gated transmission unit for the downlink DPCCH; and a pilot symbol of slot number 13 and TFCI and TPC of slot number 14 are set as a gated transmission unit for the downlink DPCCH.

<Case 2> shows a case where transmission of the uplink DPCCH goes ahead of transmission of the downlink DPCCH at the start of gated transmission. At this point, with regard to two adjacent slots, a pilot symbol of slot number 0 and TFCI and TPC of slot number 1 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 3 and TFCI and TPC of slot number 4 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 6 and TFCI and TPC of slot number 7 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 9 and TFCI and TPC of slot number 10 are set as a gated transmission unit for the downlink DPCCH; and a pilot symbol of slot number 12 and TFCI and TPC of slot number 13 are set as a gated transmission unit for the downlink DPCCH.

In FIG. 12B, <Case 3> shows a case where transmission of the uplink DPCCH goes ahead of transmission of the downlink DPCCH at the start of gated transmission. At this point, with regard to two adjacent slots, a pilot symbol of slot number 1 and TFCI and TPC of slot number 2 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 4 and TFCI and TPC of slot number 5 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 7 and TFCI and TPC of slot number 8 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 10 and

TFCI and TPC of slot number 11 are set as a gated transmission unit for the downlink DPCCH; and a pilot symbol of slot number 13 and TFCI and TPC of slot number 14 are set as a gated transmission unit for the downlink DPCCH.

<Case 4> shows a case where transmission of the uplink DPCCH goes ahead of transmission of the downlink DPCCH at the start of gated transmission. At this point, with regard to two adjacent slots, a pilot symbol of slot number 14 and TFCI and TPC of slot number 0 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 2 and TFCI and TPC of slot number 3 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 5 and TFCI and TPC of slot number 6 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 8 and TFCI and TPC of slot number 9 are set as a gated transmission unit for the downlink DPCCH; and a pilot symbol of slot number 11 and TFCI and TPC of slot number 12 are set as a gated transmission unit for the downlink DPCCH.

<Case 5> shows a case where transmission of the uplink DPCCH goes ahead of transmission of the downlink DPCCH at the start of gated transmission. At this point, with regard to two adjacent slots, a pilot symbol of slot number 0 and TFCI and TPC of slot number 1 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 3 and TFCI and TPC of slot number 4 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 6 and TFCI and TPC of slot number 7 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 9 and TFCI and TPC of slot number 10 are set as a gated transmission unit for the downlink DPCCH; and a pilot symbol of slot number 12 and TFCI and TPC of a slot number 13 are set as a gated transmission unit for the downlink DPCCH.

FIG. 12C shows gated transmission for the downlink and uplink DPCCHs according to a sixth embodiment of the present invention. FIG. 12C shows a case where the gating rate for gated transmission of the downlink and uplink DPCCHs is 1/5, i.e., gated on transmission is performed so that 1/5 of the slots are transmitted in comparison to all the slots in standard transmission. That is, gated transmission is performed so that 3 slots out of the standard 15 slots are transmitted. At this point, a gated transmission unit for the downlink DPCCH is set to be different from a slot unit. That is, with regard to two adjacent slots, a pilot symbol of the predetermined

nth slot and TFCI and TPC of the (n+1)th slot are set as a gated transmission unit for the downlink DPCCH. Accordingly, the pilot symbol, TPC symbol and TFCI symbol are transmitted in 5 slots, and the symbols are transmitted in the order of the pilot symbol of the nth slot and the TPC and TFCI symbols of the (n+1)th slot. Here, the TPC symbol and the TFCI symbol are continuously transmitted.

Referring to FIG. 12C, with regard to two adjacent slots, a pilot symbol of slot number 3 and TFCI and TPC of slot number 4 are set as a gated transmission unit for the downlink DPCCH; a pilot symbol of slot number 8 and TFCI and TPC of slot number 9 are set as a gated transmission unit for the downlink DPCCH; and a pilot symbol of slot number 13 and TFCI and TPC of slot number 14 are set as a gated transmission unit for the downlink DPCCH.

FIG. 12D shows gated transmission for the downlink and uplink DPCCHs according to a seventh embodiment of the present invention. Referring to FIG. 12D, the gating pattern is set such that the last slot of the uplink DPCCH should not be gated in the RBS mode. Such a gating pattern has high channel estimation performance, since the base station can perform channel estimation using the pilot symbols in the last slot of the frame. In addition, it is possible to increase the time required when the base station processes the FBI bits transmitted from the mobile station.

FIG. 12E shows gated transmission for the downlink and uplink DPCCHs according to an eighth embodiment of the present invention. Shown is a gating pattern for transmitting a downlink message during gated transmission in the RBS mode.

Referring to FIG. 12E, for the frame period where the downlink message is transmitted (i.e., downlink DPDCH transmission period), gated transmission is discontinued for the pilot and TFCI, and only the TPC continues to undergo gated transmission according to the gating pattern. As illustrated in FIG. 12E, for the frame period where the uplink message is transmitted (i.e., uplink DPDCH transmission period), it is also possible to stop gating the pilot and TFCI, and continuously gate the FBI and TPC according to the gating pattern.

When the mobile communication system performs the gated transmission

function according to the present invention, it is necessary to be able to control transmission power of the DPCCH data even in the gated transmission state. Herein, a description will be made of operation in which the mobile station and the base station generate and transmit a TPC bit by measuring a signal received from the other party during gated transmission, and control transmission power of the data using the received TPC bit.

Gating of the DPCCH data is started and ended at the time indicated by the upper layer. In the gated transmission mode, the base station and the mobile station have the different operation according to whether there exists the DPDCH in the DPCH to be transmitted. When the DPDCH is not included in the DPCH, the gated transmission controller of the transmission side gates on data of the selected slot in the corresponding gating slot group and gates off data of the other slots by controlling the DPCCH data. Here, the method for determining the gating position of the slots in the gating slot group unit can be performed according to a predetermined gating pattern, or the gating position of the slots can also be determined in the irregular pattern using the SFN or CFN, as described above. Otherwise, when the DPDCH data is existed in the DPCH, the transmitter transmits (or gates on) every time slot. However, the receiving side recognizes only the slot in the selected gating position out of the slots of the received frame as a valid slot in term of power control. Such gated transmission can be applied either only to the downlink between the base station and the mobile station, or both to the uplink and the downlink. Power control is differently performed for the case where the gated transmission is applied only to the downlink and for the case where the gated transmission is applied both to the uplink and the downlink.

The uplink power control includes one method in which the base station generates a TPC (Transmit Power Control) bit by measuring a communication quality of the uplink, and another method in which the mobile station controls its transmission power according to the TPC bit transmitted from the base station over the downlink. The downlink power control includes one method in which the mobile station generates a TPC bit by measuring a communication quality of the downlink, and another method in which the base station controls its transmission power according to the TPC bit transmitted from the mobile station over the uplink. In describing the power control method during gated transmission, the time point when the TPC bit is generated and transmitted and the time point when the transmission

power is controlled using the received TPC bit will be described separately from the viewpoint of the base station and the mobile station.

First, a description will be made of a power control operation for the case where the gated transmission operation is performed both on the uplink and the downlink.

When the gated transmission operation is performed on the uplink and the downlink, since the slots which can be transmitted by the base station and the mobile station exist in an irregular pattern, power control should be performed considering the irregular pattern. FIGS. 17A and 17B show the power control time relationship when the gated transmission is performed on both the uplink and the downlink

Uplink Transmission Power Control of Mobile Station

The mobile station extracts TPC bits from the valid slot last received from the base station, i.e., from the gated-on slot of the downlink, and controls transmission power of its DPCCH data according to the value of the TPC bits. Here, since the valid slot of the downlink may be different from the valid slot of the uplink according to the type of the irregular gating pattern, the mobile station stores the received valid TPC bits and then transmits a transmittable slot, if any, according to the stored TPC bits.

TPC bit Generation and Transmission for Downlink Power Control

The mobile station generates a TPC bit by measuring the communication quality of the downlink during the valid (or gated-on) slot of the downlink. The generated TPC bit is stored before transmission, until the valid uplink slot is transmitted.

Downlink Transmission Power Control of Base Station

The base station extracts TPC bits from the valid slot last received from the mobile station, i.e., from the gated-on slot of the uplink, and controls its transmission power according to the value of the TPC bits. Here, since the valid slot of the uplink may be different from the valid slot of the downlink according to the

type of the irregular gating pattern, the mobile station stores the received valid TPC bits and then transmits a transmittable slot, if any, according to the stored TPC bits.

TPC Bit Generation and Transmission for Uplink Power Control

The base station generates a TPC bit by measuring the communication quality of the uplink during the valid slot of the uplink. The generated TPC bit is stored before transmission, until the valid downlink slot is transmitted.

Next, a description will be made of a power control operation for the case where the gated transmission is applied only to the downlink in the mobile communication system having the gated transmission function.

In the mobile communication system, when the gated transmission is applied only to the downlink, the mobile station continuously transmits the DPCCH data, whereas the base station transmits only the slot data in the gating position selected in the gating slot group unit. Therefore, the base station should perform a power control method being different from that for the case where the base station and the mobile station both perform the gated transmission, since the transmittable slots exist in the irregular pattern. FIGS. 18A and 18B show the power control time relationship for the case where the gated transmission is applied only to the downlink

Uplink Transmission Power Control of Mobile Station

The mobile station extracts TPC bits from the valid slot last received from the base station, i.e., from the slot in the gating position of the downlink selected in the gating slot group unit, and controls its transmission power according to the value of the TPC bits. Here, since the valid slot of the downlink may be different from the valid slot of the uplink according to the type of the irregular gating pattern, the mobile station stores the received valid TPC bits and then transmits a transmittable slot, if any, according to the stored TPC bits.

TPC Bit Generation and Transmission for Downlink Power Control

The mobile station generates a TPC bit by measuring the communication quality of the downlink during the valid slot of the downlink. The mobile station

immediately transmits the generated TPC bit to the base station, and repeatedly transmits the TPC bit until a new TPC bit is generated. The reason for repeatedly transmitting the TPC bit is because the base station receives at least one TPC bit until the slot where the base station can transmit the downlink, and it is possible to decrease a TPC error rate by repeated transmission.

Downlink Transmission Power Control of Base Station

The base station extracts TPC bits received from the mobile station and controls its transmission power according to the value of the TPC bits. Here, the base station can extract the TPC bits using at least one TPC bit repeatedly transmitted by the mobile station.

As described above, in the embodiment of the present invention, it is possible to control transmission power the base station and the mobile station not only for the case where the uplink DPCCH signal is gated and the downlink DPCCH signal is not gated or the downlink DPCCH signal is gated and the uplink DPCCH signal is not gated, but also for the case where both the uplink and downlink DPCCH data is gated.

As described above, the invention can increase system capacity by minimizing the time required in the sync reacquisition process of the base station, decreasing interference due to discontinuous transmission of the uplink DPCCH, increasing the mobile station battery life time, and decreasing interference due to transmission of the uplink TPC bits.

While the invention has been shown and described with reference to a certain preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method for transmitting control data on a downlink channel in a base station for a mobile communication system, comprising the steps of:

determining whether the base station has downlink and uplink traffic channel data;

driving, if there is no traffic data for a predetermined time period, a random position selector to determine a random gating slot position;

gating on control data at the determined gating slot position; and

gating off control data in other slot positions.

2. The method as claimed in claim 1, wherein the channel data comprises a series of frames, each frame includes a plurality of slots, slots in each frame are divided into a plurality of gating slot groups, and each gating slot group has a determined gating slot position.

3. The method as claimed in claim 2, wherein the frame is comprised of 15 slots, the slot group is comprised of 5 slots, and the determined slot position is a randomized slot position out of the slots in the slot group.

4. The method as claimed in claim 2, wherein the frame is comprised of 15 slots, and each gating slot group is comprised of 3 slots.

5. The method as claimed in claim 2, wherein the random position selector determines the gating slot position by:

calculating a value x by multiplying a system frame number (SFN) of a immediately before the transmission by a specific integer;

selecting N bits, said N bits being selected starting from a position which is at an x-chip distance from a start point of a scrambling code of previous gating slot group ; and

determining a gating slot position of the each gating slot group by performing a modulo operation on the selected n bits, said modulo operation being by a number of slots in the gating slot group.

6. The method as claimed in claim 2, wherein the random position

selector determines the gating slot position using the following equation:

$$N(G,C^i)=\left(\sum_{l=0}^{15}\left(S\left(G_{prev}\times 2560\times\frac{1}{T}+G_{prev}+l\right)\oplus C^i_{(k \bmod 8)}\right)\times 2^{15-l}\right)\bmod T$$

where, G is a gating slot group number;

G_{prev} is a previous gating slot group number;

C^i is a Connection Frame Number (CFN) of an ith frame $(=(C^i_0C^i_1C^i_2C^i_3C^i_4C^i_5C^i_6C^i_7)_2)$; and

T is a reciprocal of the gating rate.

7. The method as claimed in claim 2, wherein the random position selector determines the gating slot position using the following equation except for the first gating slot group and last gating slot group:

$$s(i,j)=(A_j\oplus C_i)\bmod S_G,\qquad j=0,1,2,.,,,.N_G-1,\qquad i=0,1,...,255$$

where, A_j is a sequence obtained by applying j bit offset to a fixed sequence;

C_i is a sequence obtained by repeating a Connection Frame Number (CFN);

S_G is a number of slots in one gating slot group; and

N_G is a number of gating slot groups in one frame.

8. The method as claimed in claim 7, wherein the random position selector determines the gating slot position of the first gating slot group except for the first slot.

9. The method as claimed in claim 8, wherein the random position selector determines the gating slot position of the last gating slot group as the last slot.

10. The method as claimed in claim 2, wherein the gating on control data includes a pilot symbol and a TPC (Transmit Power Control) bit.

11. The method as claimed in claim 2, wherein the gating on control data includes a TPC (Transmit Power Control) bit located in the determined gating slot position and a pilot symbol located in a slot previous to the determined gating slot position.

12. The method as claimed in claim 1, wherein the base station transmits, if there is no data on the downlink and uplink traffic channel for the predetermined time period, gating information includes a gating start time and a gating rate.

13. A method for transmitting control data on an uplink channel in a mobile station for a mobile communication system, comprising the steps of:

determining whether the mobile station has uplink traffic channel data to transmit to a base station;

transmitting, if there is no data to be transmitted over the uplink data channel for a predetermined time period, a request for gating uplink control data to the base station;

driving, when the mobile station receives gating information including gating start time and gating rate from the base station, a random position selector to determine a random gating slot position;

gating on control data in the determined slot position; and

gating off control data in other slot positions.

14. A method for gating data using a plurality of slots in an ith frame in a stream of frames, wherein each frame includes a plurality of slots and the slots in each frame are divided into a plurality of gating slot groups, each gating slot group including a plurality of slots, the method comprising the step of:

transmitting data in a slot position determined by Equations (1)-(3) below,

$$s(i,j)=\begin{cases}(A_j \oplus C_i)\bmod(S_G-1)+1, & j=0 & (1)\\ (A_j \oplus C_i)\bmod S_G, & j=1,2,...,N_G-2, \quad i=0,1,...,255 & (2)\\ S_G-1, & j=N_G-1 & (3)\end{cases}$$

where j is a number of a gating slot group in the ith frame;

where C_i is a sequence obtained by repeating a ith connection frame number(CFN); and

where A_j is a sequence associated with a jth gating slot group, said sequence obtained by applying j bit offset to a given sequence;

where S_G is a number of slots in one gating slot group; and

where N_G is a number of gating slot groups in one frame .

15. A method for gating data using a plurality of slots in an ith frame in a stream of frames, wherein each frame includes a plurality of slots and the slots in each frame are divided into a plurality of gating slot groups, each gating slot group including a plurality of slots, the method comprising the steps of:

determining a gating slot position of gating slot groups using the gating slot position formula below:

$$s(i,j) = (A_j \oplus C_i) \bmod S_G, \qquad j = 0,1,2,..,,,N_G - 1$$

where s(i,j) is a slot position within a jth gating slot group in a ith frame;

where j is a number of a gating slot group in an ith frame;

where C_i is a sequence obtained by repeating the ith frame number(CFN); and

where A_j is a sequence associated with a jth gating slot group, said sequence obtained by applying j bit offset to a given sequence;

gating on Transmit Power Control (TPC) bit at the determined gating slot position; and

gating off the TPC bit at other slots.

16. The method as claimed in claim 15, wherein the gating on step comprises the steps of:

gating on the TPC bit at the determined gating slot position ; and

gating on a pilot symbol at a slot located before the determined gating slot position.

17. The method as claimed in claim 15, wherein the gating slot position determination step further comprises the step of:

determining a gating slot position in a first gating slot group of an ith frame by using a formula below:

$$s(i,j) = (A_j \oplus C_i) \bmod (S_G - 1) + 1, \qquad j = 0 \qquad i = 0,1,...,255$$

18. The method as claimed in claim 15, wherein the gating slot position determination step further comprises the step of:

determining a gating slot position in a last gating slot group of an ith frame as last slot.

19. A method for transmitting gated transmission of uplink dedicated physical control channel(DPCCH) data which is formed by series of frames, the frame includes plurality of slots, for a mobile communication system, comprising the steps of:

receiving a gating information indicating gating start time and gating rate from a base station;

transmitting the DPCCH slot signal to form a random pattern for a predetermined duration.

20. A method as claimed in claim 19, wherein the random pattern is generated by determining gating on slot position using bellow equation;

$$s(i,j)=\begin{cases}(A_j \oplus C_i)\bmod(S_G-1)+1, & j=0 & (1)\\ (A_j \oplus C_i)\bmod S_G, & j=1,2,...,N_G-2, \quad i=0,1,...,255 & (2)\\ S_G-1, & j=N_G-1 & (3)\end{cases}$$

where, where j is a number of a gating slot group in the ith frame;

where C_i is a sequence obtained by repeating the ith frame number; and

where A_j is a sequence obtained by applying j bit offset to a given sequence;

where S_G is a number of slots in one gating slot group; and

where N_G is a number of gating slot groups in one frame .

21. A base station transmitter in a mobile communication system, in which traffic channel data and dedicated physical control channel (DPCCH) data each are comprised of a series of frames, and each frame includes a plurality of slots, comprising:

a gating position selector for determining a gating slot position when there is no data to transmit on the traffic channel for a predetermined time period, and for dividing the slots in each frame into a plurality of gating slot groups, each of said gating slot groups having a random gating slot position;

a gated transmission controller for controlling a DPCCH slot corresponding

to the selected gating slot position.

22. The base station transmitter as claimed in claim 21, wherein the gating position selector determining the gating slot positionby using formulas (1)-(3) below:

$$s(i,j)=\begin{cases}(A_j \oplus C_i)\bmod(S_G-1)+1, & j=0 & (1)\\ (A_j \oplus C_i)\bmod S_G, & j=1,2,...,N_G-2, \quad i=0,1,...,255 & (2)\\ S_G-1, & j=N_G-1 & (3)\end{cases}$$

where j is a number of a gating slot group in the ith frame;

where C_i is a sequence obtained by repeating the ith frame number (CFN=i); and

where A_j is a sequence associated with a jth gating slot group, said sequence obtained by applying j bit offset to a given sequence;

where S_G is a number of slots in one gating slot group; and

where N_G is a number of gating slot groups in one frame.

23. The base station transmitter as claimed in claim 21, wherein the gating position selector determining the gating slot positionby using a formula below:

$$s(i,j)=(A_j \oplus C_i)\bmod S_G, \qquad j=0,1,2,.,,,.N_G-1, \qquad i=0,1,...,255$$

where s(i,j) is a slot position within a jth gating slot group in a ith frame;

where j is a number of a gating slot group in the ith frame;

where C_i is a sequence obtained by repeating the ith frame number; and

where A_j is a sequence associated with a jth gating slot group in the ith frame, said sequence obtained by applying j bit offset to a given sequence.

24. The base station transmitter as claimed in claim 21, wherein the gating position selector determining the gating slot positionby using a formula below:

$$s(i,j) = (A_j \oplus C_i) \bmod (S_G - 1) + 1, \qquad j = 0 \qquad i = 0,1,...,255$$

where s(i,j) is a slot position within a jth gating slot group in a ith frame;

where j is a number of a gating slot group in the ith frame;

where C_i is a sequence obtained by repeating the ith frame number; and

where A_j is a sequence associated with the jth gating slot group, said sequence obtained by applying j bit offset to a given sequence.

25. The base station transmitter as claimed in claim 21, wherein the gating position selectordetermining the gating slot positionby using a formula below:

$$s(i,j) = S_G - 1, \qquad j = N_G - 1, \qquad i = 0,1,...,255$$

where s(i,j) is a slot position within a jth gating slot group in a ith frame;

where j is a number of a gating slot group in the ith frame;

where C_i is a sequence obtained by repeating the ith frame number; and

where A_j is a sequence associated with a jth gating slot group, said sequence obtained by applying j bit offset to a given sequence.

26. The base station transmitter as claimed in claim 22, wherein the gated transmission controller gates on a pilot symbol at a slot located before a determined gating slot, and gates on at least one Transmit Power Control (TPC) bit and at least one Transport Format Combination Indicator (TFCI) bit at the determined gating slot.

27. A mobile station transmitter in a mobile communication system, in which traffic channel data and dedicated physical control channel (DPCCH) data each includes a series of frames, and each frame includes a plurality of slots, comprising:

a gating slot position selector for determining a gating slot position when the mobile station receives gating information includes gating start time and gating rate

form a base station, and dividing the slots in each frame into a plurality of gating slot groups, each of said gating slot groups having the gating slot position;

a gated transmission controller for gating on at the determined gating slot position and gating off the other slot signal in a gating slot group.

28. An apparatus for gating data of a plurality of slots in an ith frame in a series of frames, wherein each frame includes a plurality of slots and the slots in each frame are divided into a plurality of gating slot groups, each gating slot group including a plurality of slots, the apparatus comprising:

a first memory for storing a sequence C_I, said sequence obtained by repeating the ith frame number;

a second memory for storing a sequence A_j associated with a jth gating slot group, said sequence A_j obtained by a given sequence;

a multiplier for performing an exclusive-or operation on the sequences C_i and A_j;

a modulo operator for performing a modulo operation on an output of the multiplier, said modulo operation being by a number of slots in a gating slot group, where the result is a gating slot position in the jth gating slot group; and

a gated transmission controller for gating on the data in the determined gating slot position and gating off the other slot data in the gating slot group.

29. The apparatus as claimed in claim 28, wherein the gated transmission controller transmits Transmit Power Control (TPC) bit at the determined gating slot position, and a pilot symbols of a slot located before the determined gating slot position.

30. The apparatus as claimed in claim 27, wherein the modulo operator determines the gating slot position of the first gating slot groupas one of the slot in the first gating slot group except for the first slot.

31. The apparatus as claimed in claim 28, wherein the modulo operator determines the gating positionof the last gating slot group as last slot.

FIG. 1A

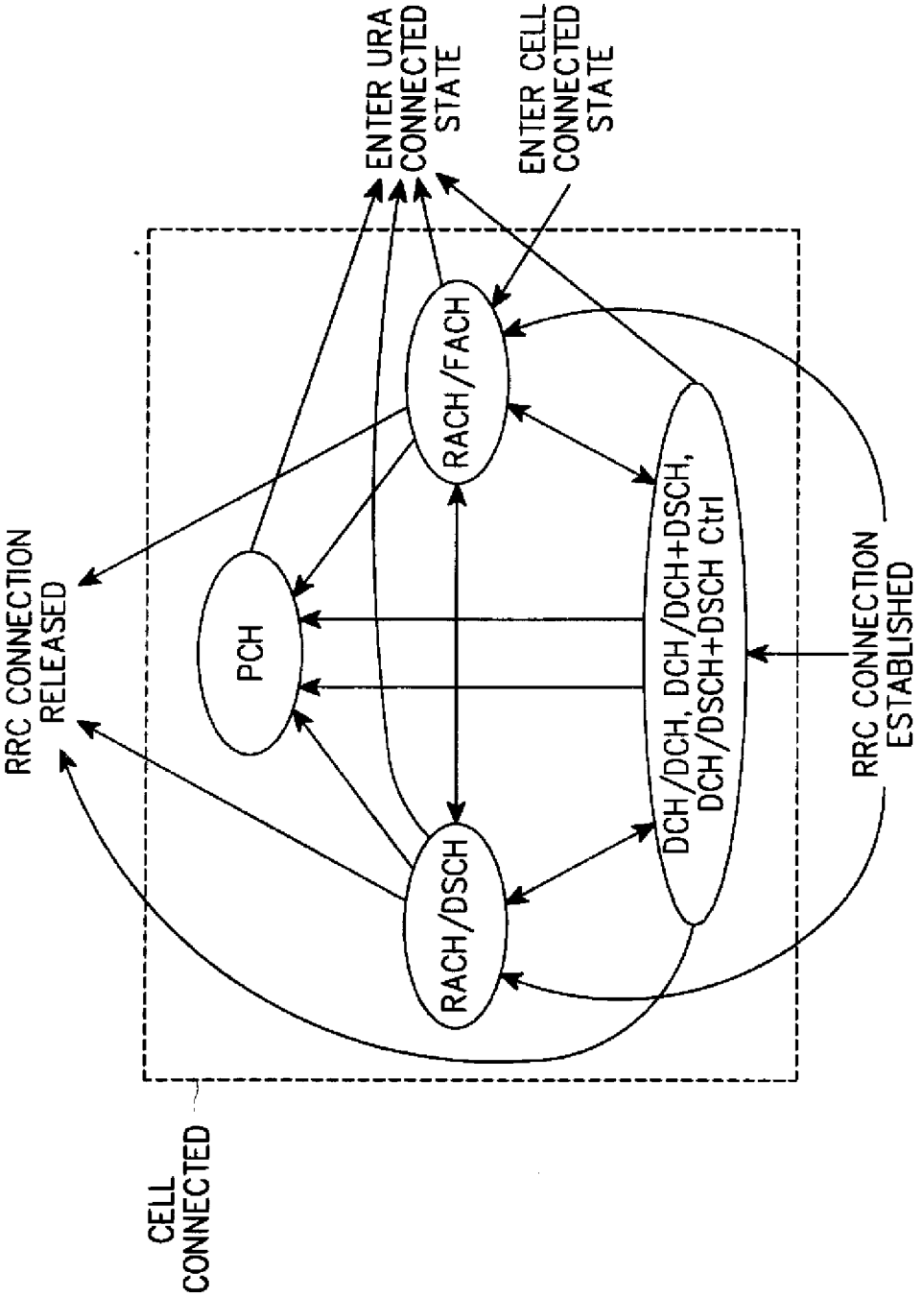

CELL CONNECTED
RRC CONNECTION RELEASED
ENTER URA CONNECTED STATE
ENTER CELL CONNECTED STATE
RRC CONNECTION ESTABLISHED
PCH
RACH/FACH
RACH/DSCH
DCH/DCH, DCH/DCH+DSCH, DCH/DSCH+DSCH Ctrl

FIG. 1B

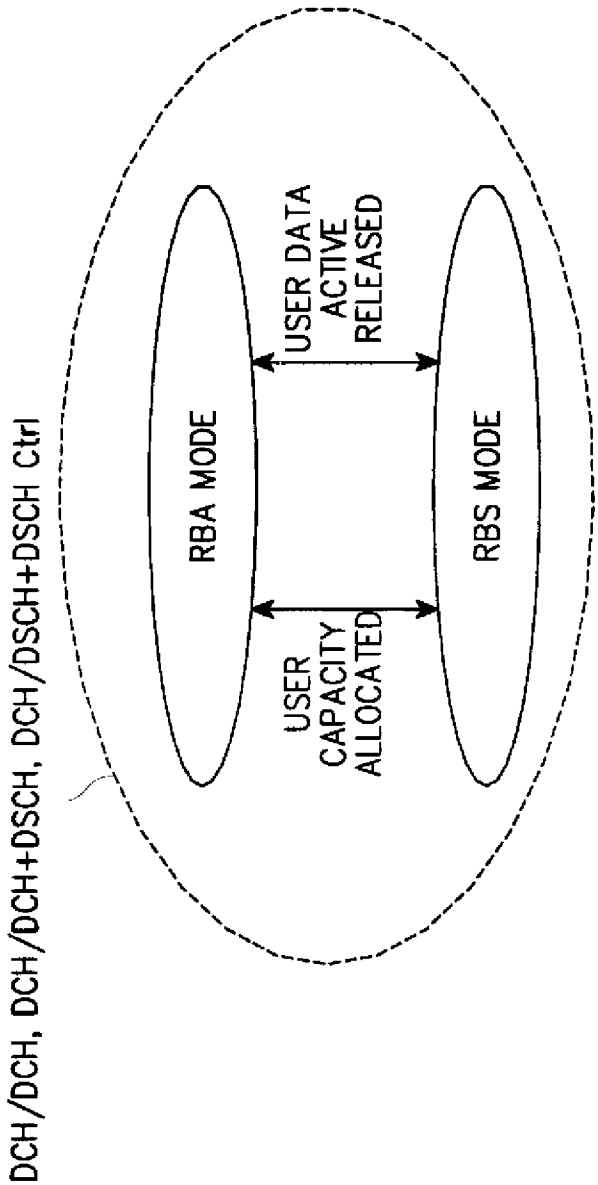

DCH/DCH, DCH/DCH+DSCH, DCH/DSCH+DSCH Ctrl
RBA MODE
USER DATA ACTIVE RELEASED
USER CAPACITY ALLOCATED
RBS MODE

FIG. 2A

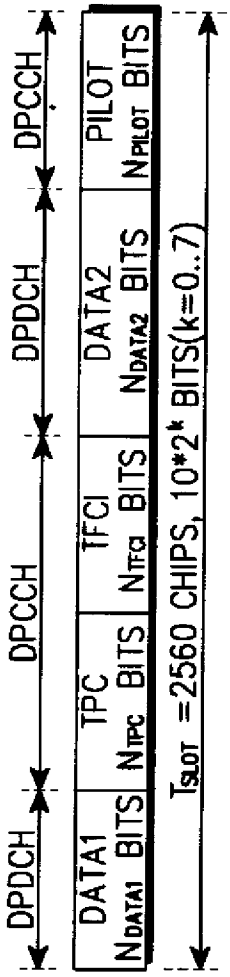

DPDCH
DPCCH
DPDCH
DPCCH
DATA1
NDATA1 BITS
TPC
NTPC BITS
TFCI
NTFCI BITS
DATA2
NDATA2 BITS
PILOT
NPILOT BITS
TSLOT =2560 CHIPS, 10*2k BITS(k=0..7)

FIG. 2B

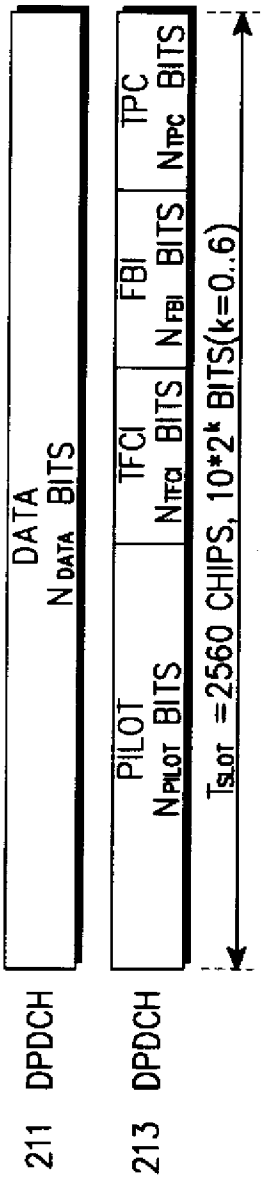

211 DPDCH
DATA
NDATA BITS
213 DPDCH
PILOT
NPILOT BITS
TFCI
NTFCI BITS
FBI
NFBI BITS
TPC
NTPC BITS
TSLOT =2560 CHIPS, 10*2k BITS(k=0..6)

FIG. 3A

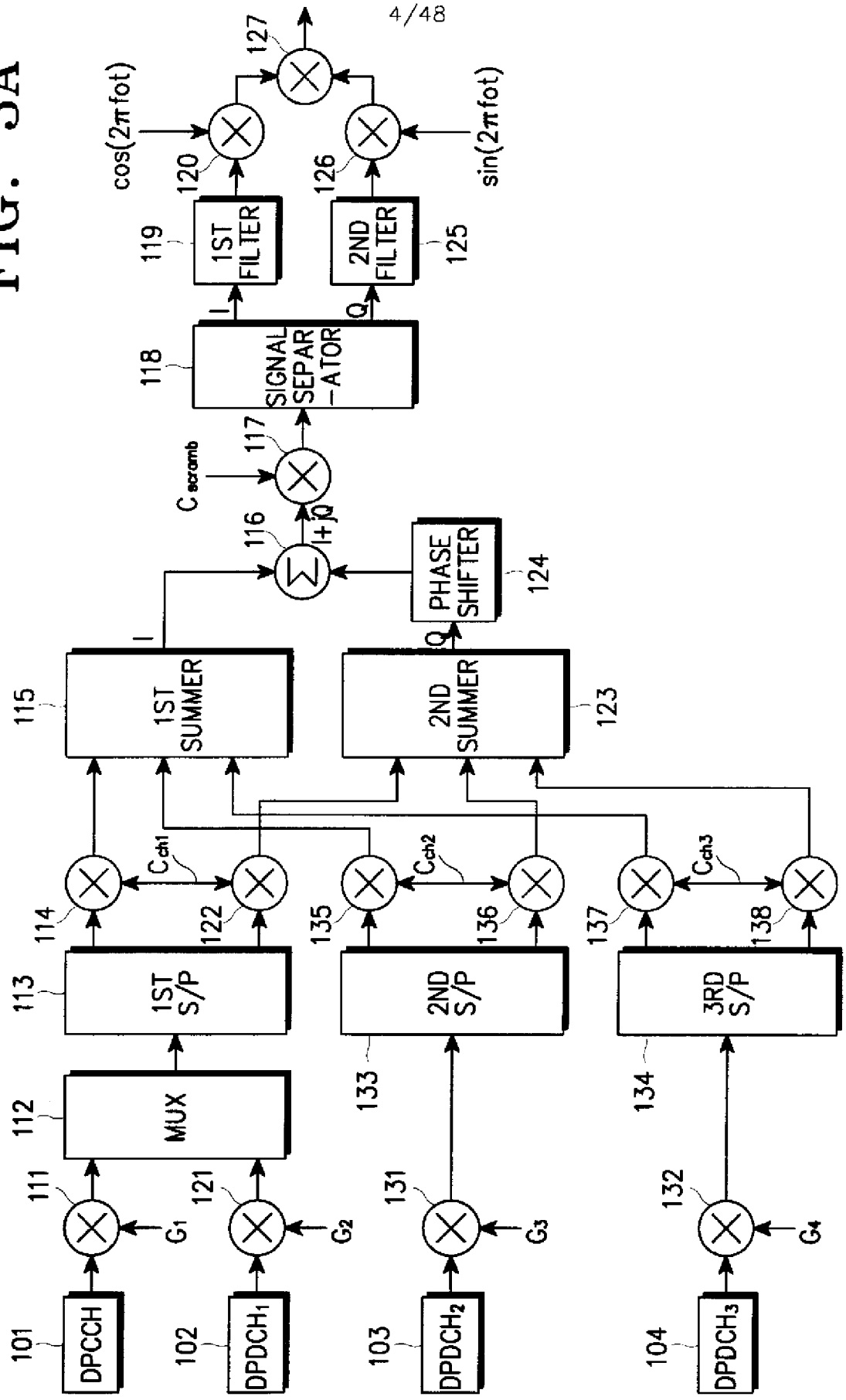

101 DPCCH
102 DPDCH1
103 DPDCH2
104 DPDCH3
111
121
131
132
G1
G2
G3
G4
112 MUX
133
134
113 1ST S/P
2ND S/P
3RD S/P
114
122
135
136
137
138
Cch1
Cch2
Cch3
115 1ST SUMMER
2ND SUMMER 123
I
Q
116
I+jQ
PHASE SHIFTER 124
Cscramb
117
118 SIGNAL SEPAR-ATOR
119 1ST FILTER
2ND FILTER 125
120
126
cos(2πfot)
sin(2πfot)
127

FIG. 3B

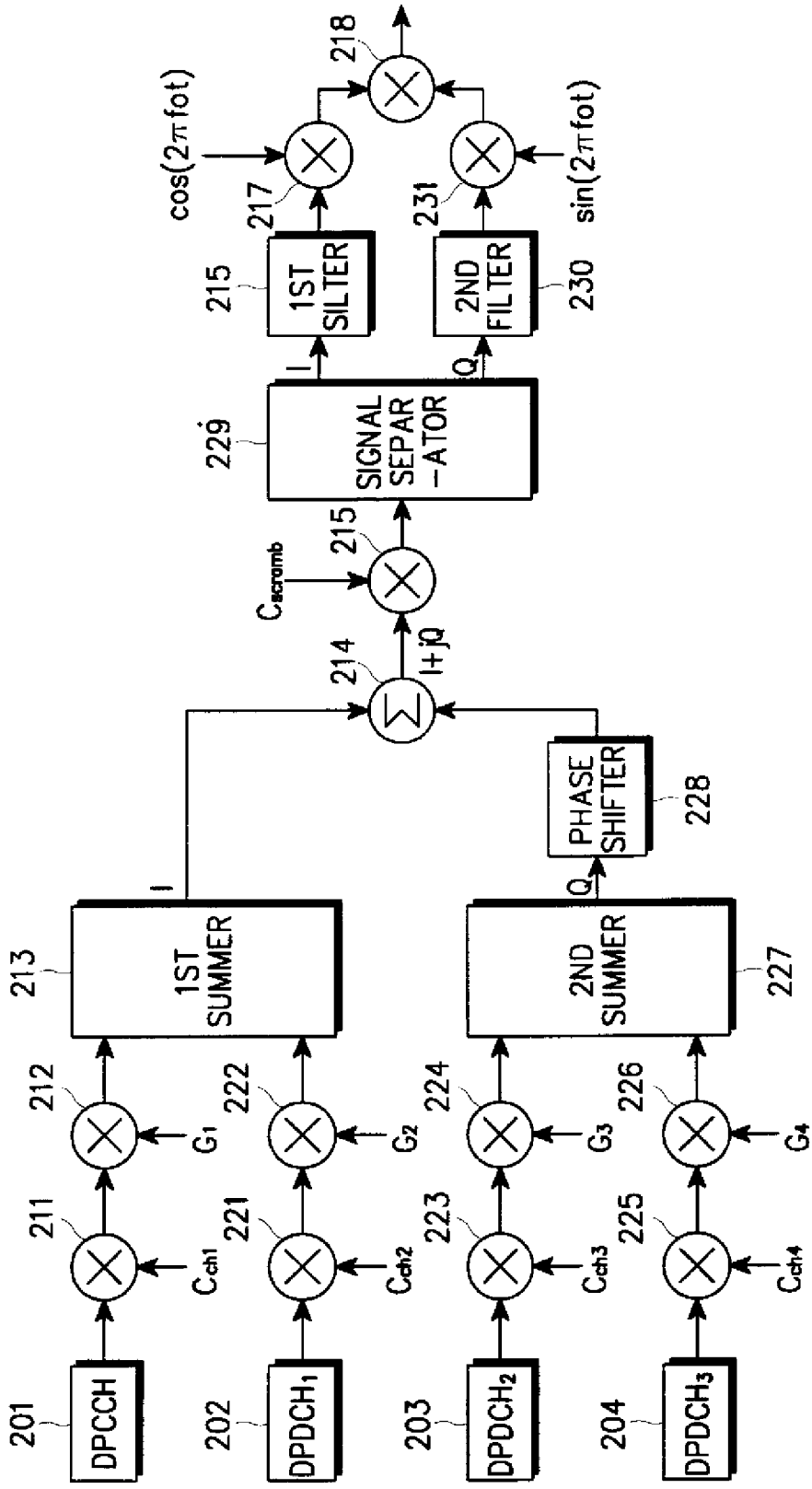

201
DPCCH
202
DPDCH1
203
DPDCH2
204
DPDCH3
211
221
223
225
212
222
224
226
G1
G2
G3
G4
Cch1
Cch2
Cch3
Cch4
213
1ST SUMMER
227
2ND SUMMER
I
Q
228
PHASE SHIFTER
214
I+jQ
215
Cscramb
229
SIGNAL SEPAR-ATOR
215
1ST SILTER
230
2ND FILTER
217
231
218
cos(2πfot)
sin(2πfot)

FIG. 4A

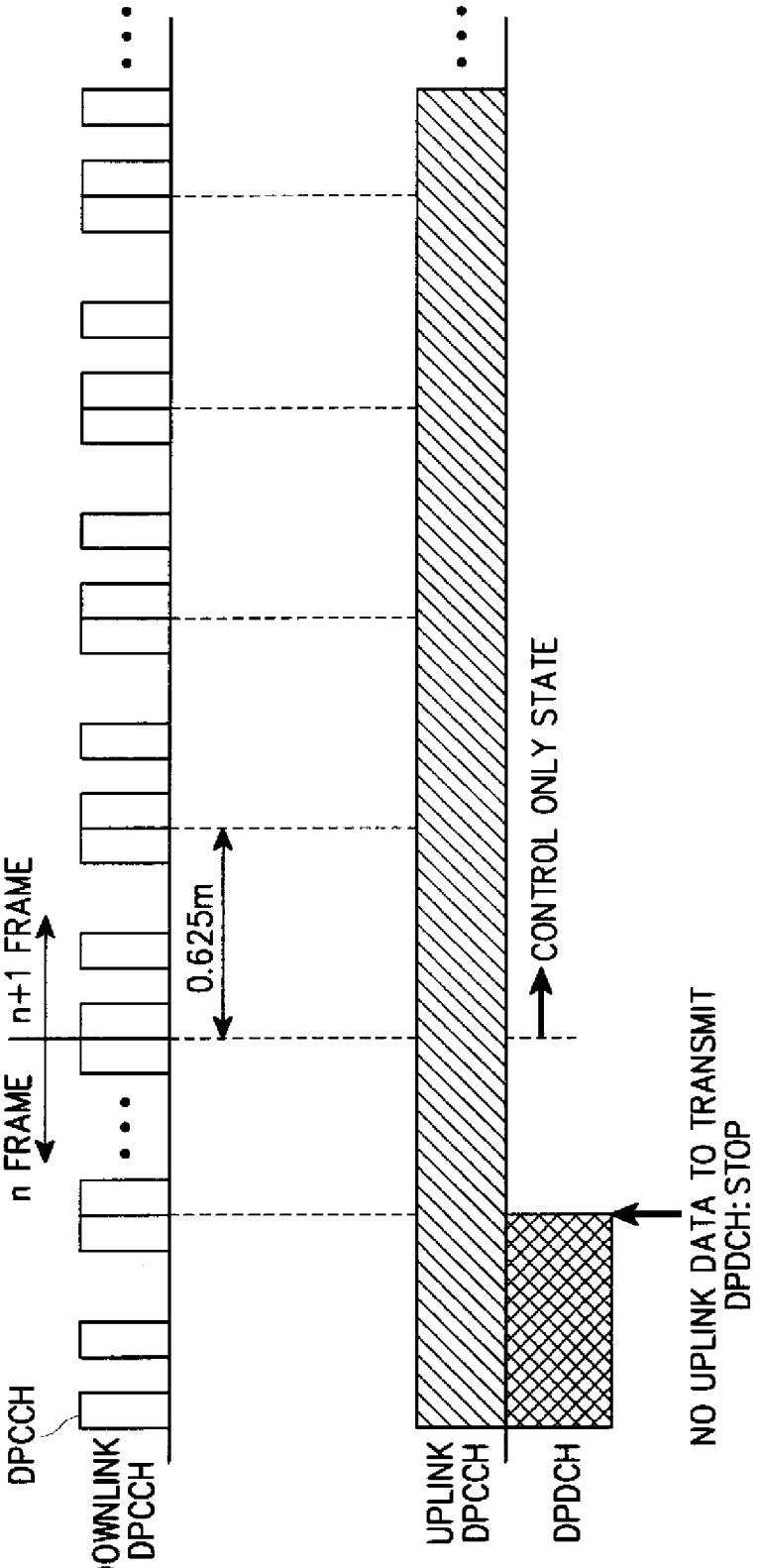

DPCCH
DOWNLINK DPCCH
n FRAME
n+1 FRAME
0.625m
UPLINK DPCCH
DPDCH
CONTROL ONLY STATE
NO UPLINK DATA TO TRANSMIT
DPDCH: STOP

FIG. 4B

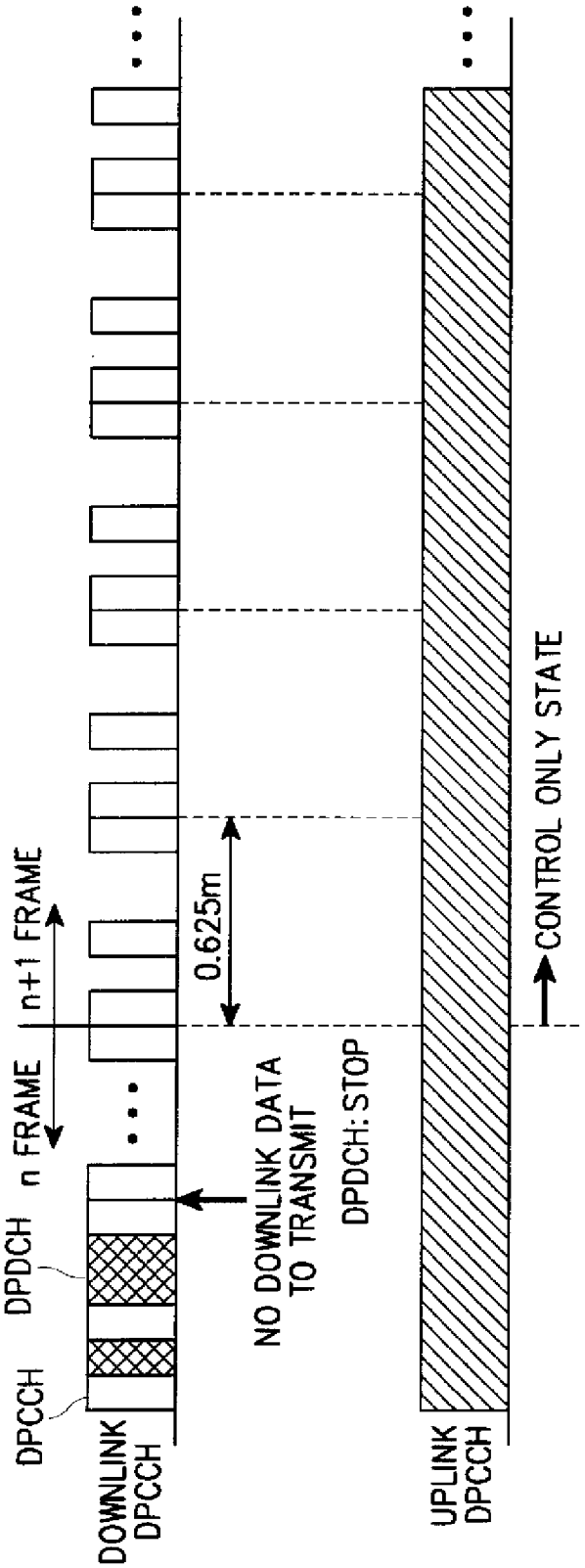

DOWNLINK DPCCH
DPCCH
DPDCH
n FRAME
n+1 FRAME
0.625m
NO DOWNLINK DATA TO TRANSMIT
DPDCH: STOP
UPLINK DPCCH
CONTROL ONLY STATE

FIG. 5A

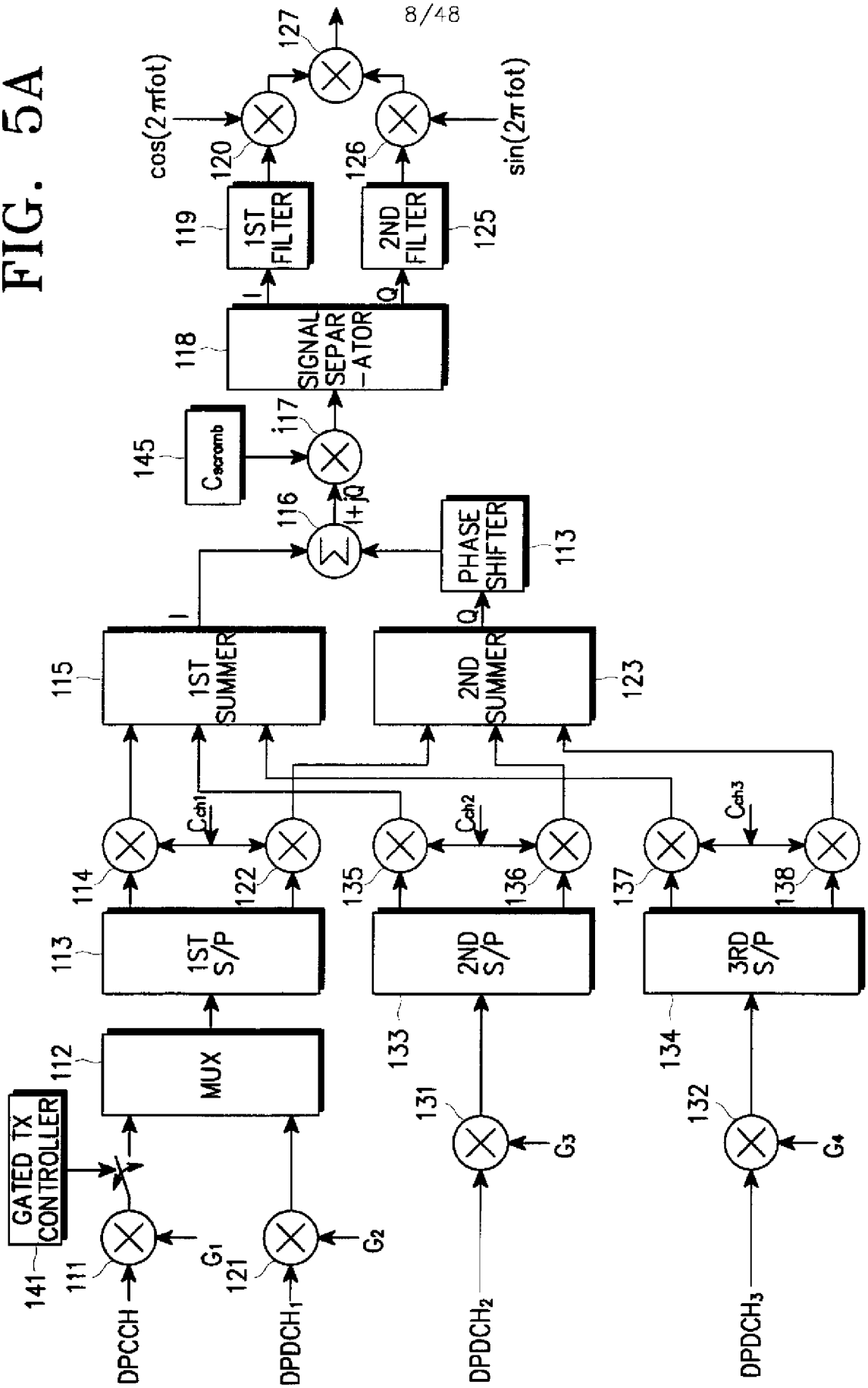

DPCCH
DPDCH1
DPDCH2
DPDCH3
G1
G2
G3
G4
111
121
131
132
141
GATED TX CONTROLLER
112
MUX
113
1ST S/P
133
2ND S/P
134
3RD S/P
114
122
135
136
137
138
Cch1
Cch2
Cch3
115
1ST SUMMER
123
2ND SUMMER
116
1+jQ
113
PHASE SHIFTER
145
Cscramb
117
118
SIGNAL SEPAR-ATOR
I
Q
119
1ST FILTER
125
2ND FILTER
120
126
cos(2πfot)
sin(2πfot)
127

FIG. 5B

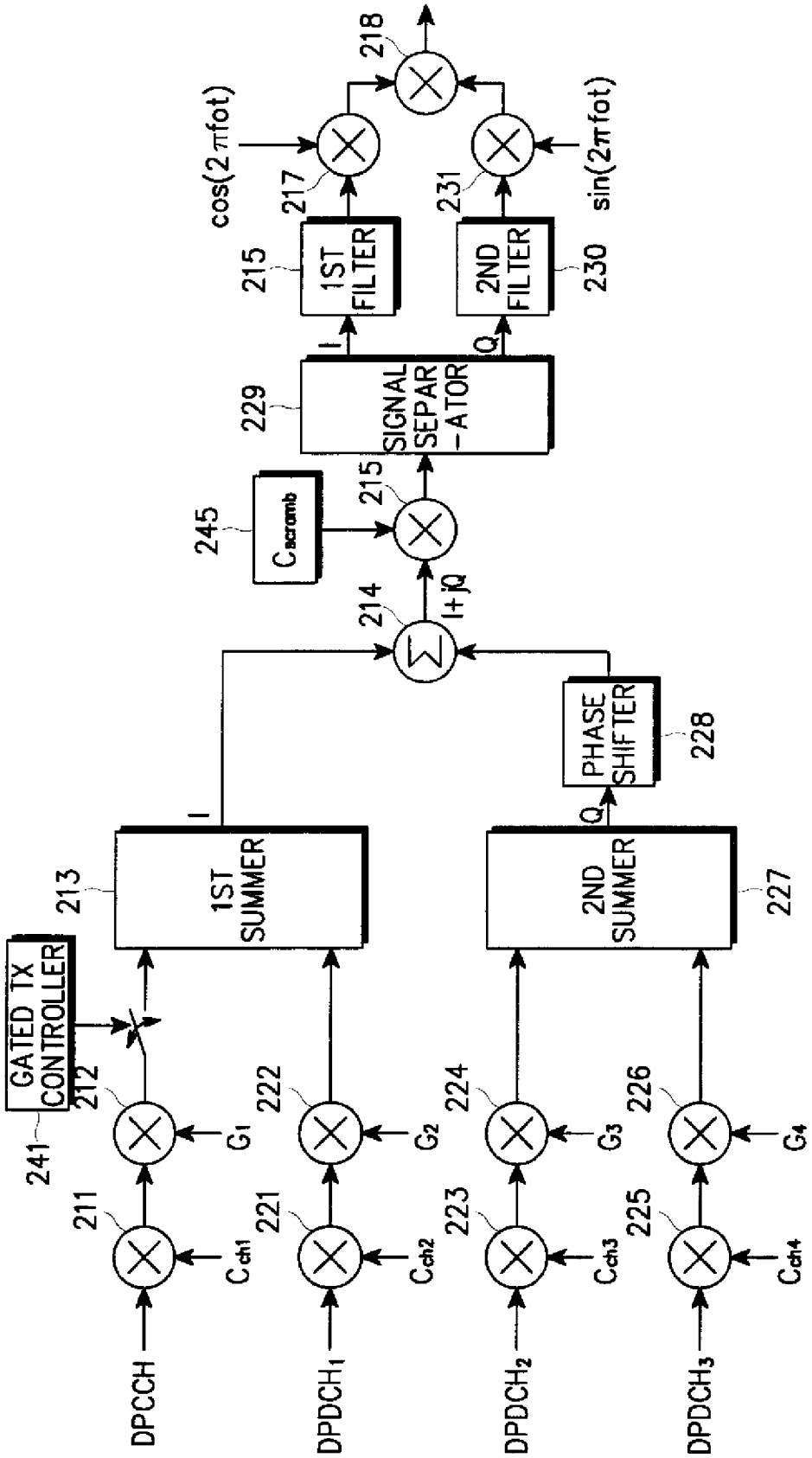

DPCCH
DPDCH1
DPDCH2
DPDCH3
Cch1
Cch2
Cch3
Cch4
211
221
223
225
241
GATED TX CONTROLLER
212
G1
222
G2
224
G3
226
G4
213
1ST SUMMER
227
2ND SUMMER
228
PHASE SHIFTER
I
Q
214
I+jQ
245
Cscramb
215
229
SIGNAL SEPAR-ATOR
215
217
1ST FILTER
230
231
2ND FILTER
218
cos(2πfot)
sin(2πfot)

FIG. 5C

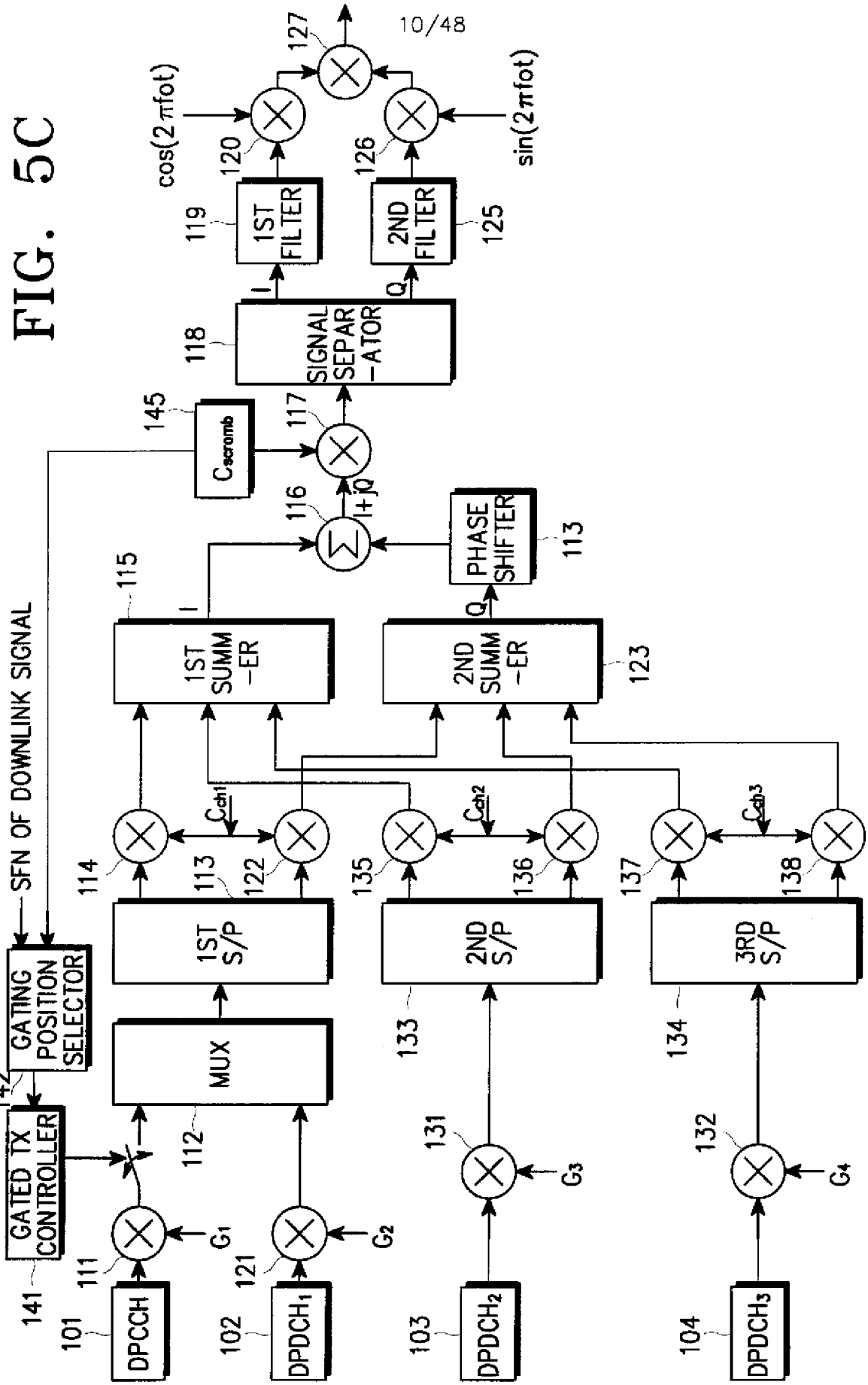

DPCCH
DPDCH1
DPDCH2
DPDCH3
101
102
103
104
111
121
131
132
G1
G2
G3
G4
141
GATED TX CONTROLLER
142
GATING POSITION SELECTOR
SFN OF DOWNLINK SIGNAL
112
MUX
1ST S/P
2ND S/P
3RD S/P
113
133
134
114
122
135
136
137
138
Cch1
Cch2
Cch3
1ST SUMM -ER
2ND SUMM -ER
115
123
I
Q
116
I+jQ
PHASE SHIFTER
113
145
Cscramb
117
118
SIGNAL SEPAR -ATOR
119
120
126
125
1ST FILTER
2ND FILTER
cos(2πfot)
sin(2πfot)
127

FIG. 5D

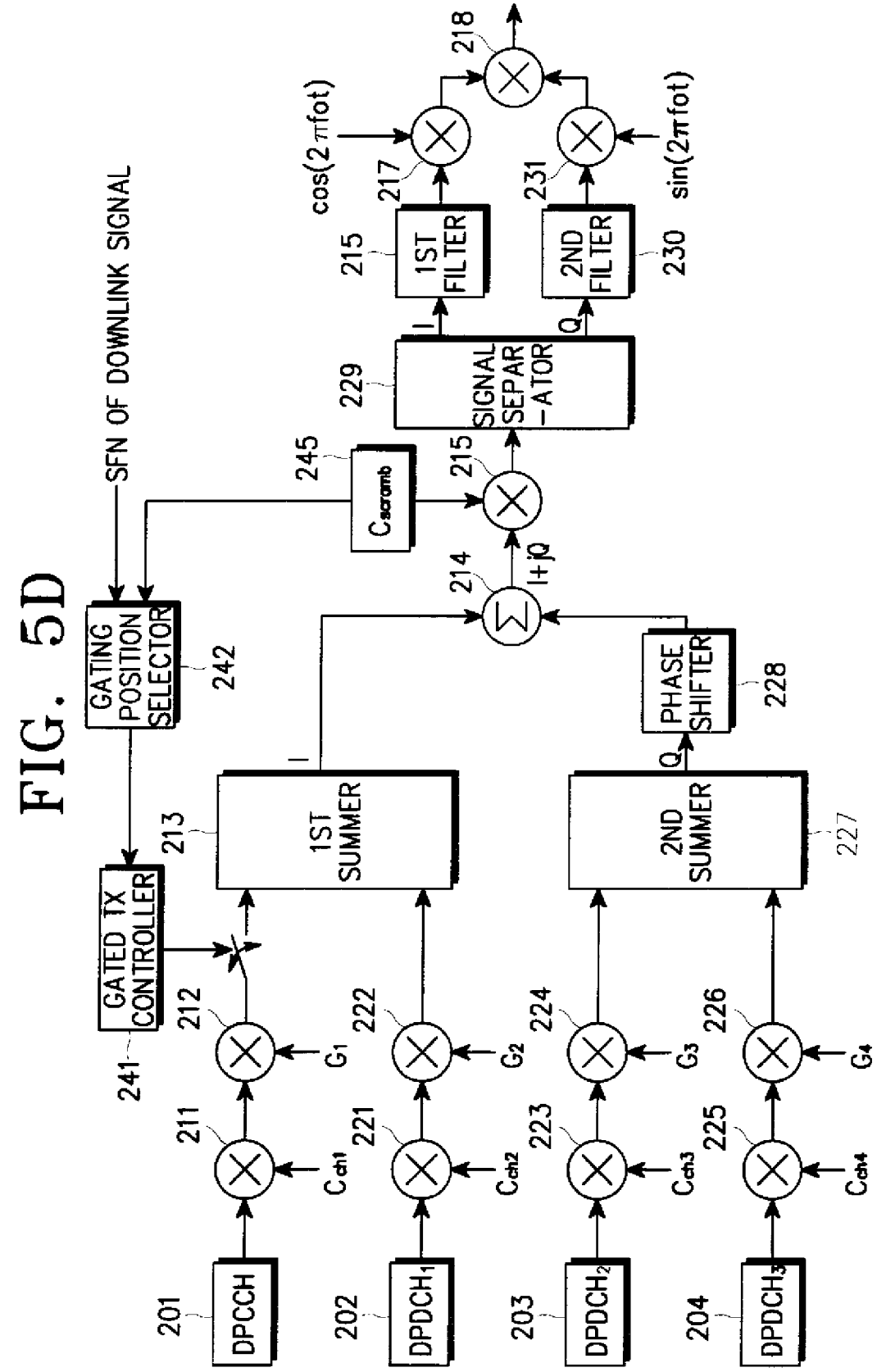

SFN OF DOWNLINK SIGNAL
GATING POSITION SELECTOR
242
GATED TX CONTROLLER
241
DPCCH
201
DPDCH1
202
DPDCH2
203
DPDCH3
204
Cch1
Cch2
Cch3
Cch4
211
221
223
225
G1
G2
G3
G4
212
222
224
226
1ST SUMMER
213
2ND SUMMER
227
PHASE SHIFTER
228
I
Q
214
I+jQ
215
Cscramb
245
SIGNAL SEPAR-ATOR
229
1ST FILTER
215
2ND FILTER
230
217
231
cos(2πfot)
sin(2πfot)
218

FIG. 6A

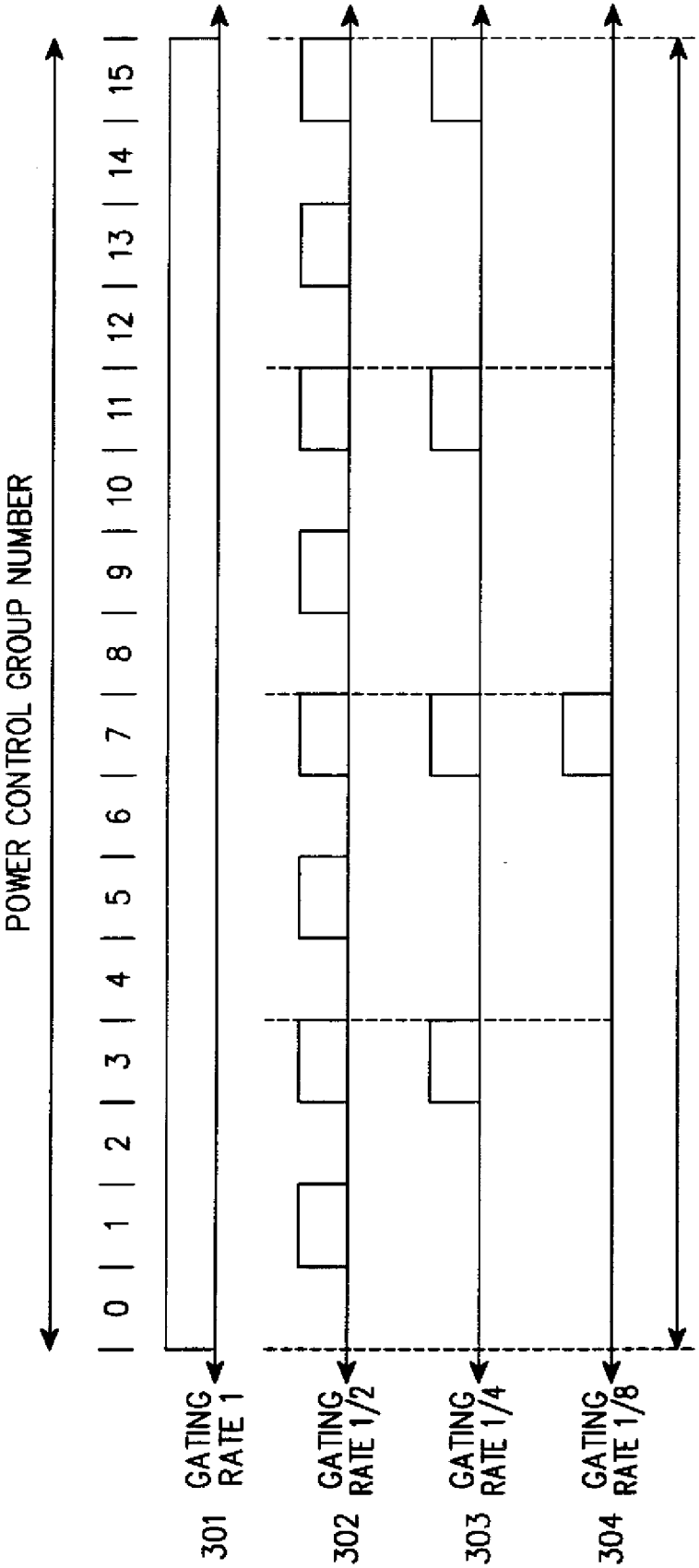

POWER CONTROL GROUP NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
301 GATING RATE 1
302 GATING RATE 1/2
303 GATING RATE 1/4
304 GATING RATE 1/8

FIG. 6B

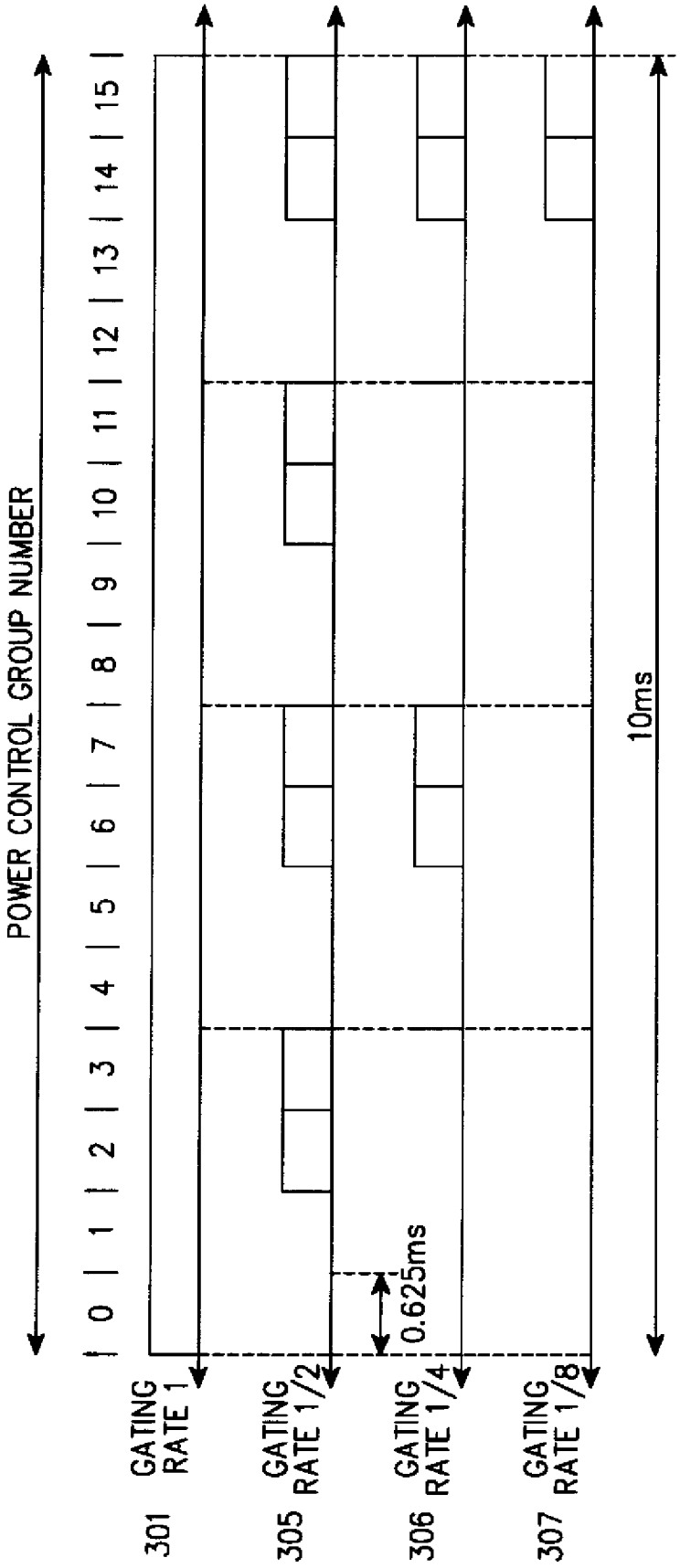

POWER CONTROL GROUP NUMBER
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
10ms
0.625ms
301 GATING RATE 1
305 GATING RATE 1/2
306 GATING RATE 1/4
307 GATING RATE 1/8

FIG. 7A

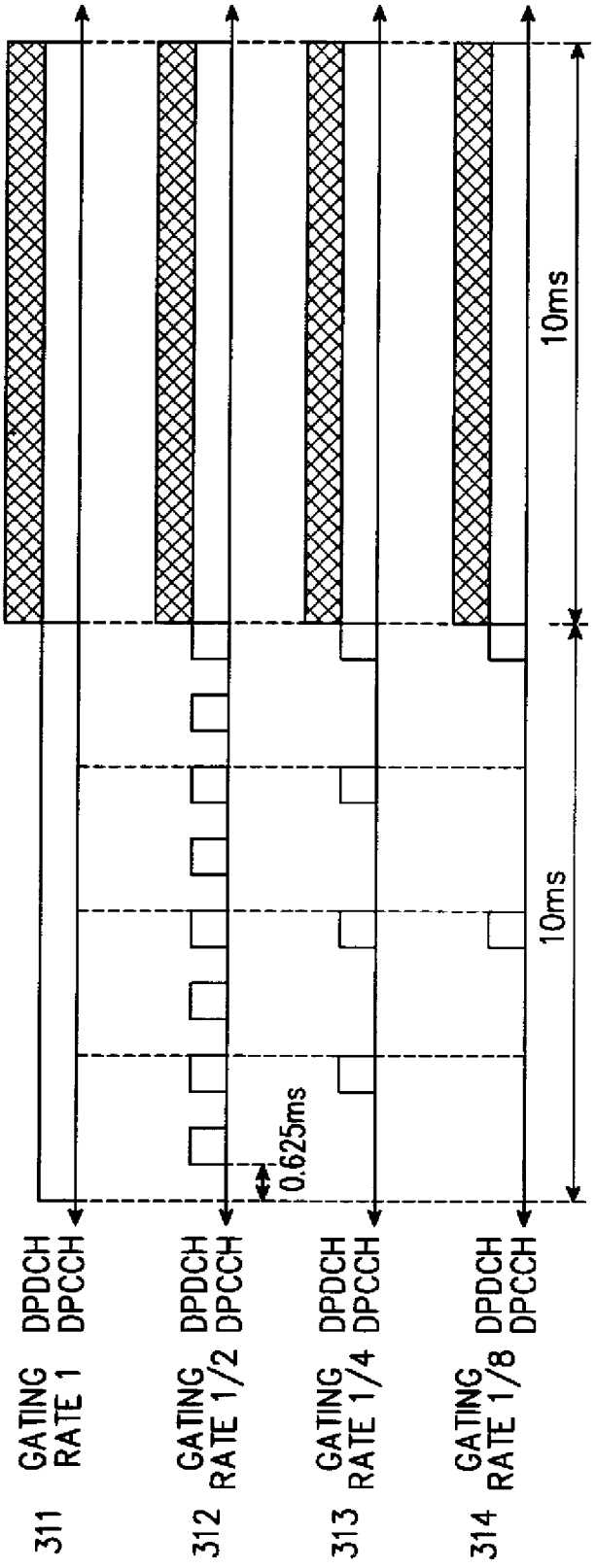

311
GATING RATE 1
DPDCH
DPCCH
312
GATING RATE 1/2
DPDCH
DPCCH
313
GATING RATE 1/4
DPDCH
DPCCH
314
GATING RATE 1/8
DPDCH
DPCCH
0.625ms
10ms
10ms

FIG. 7B

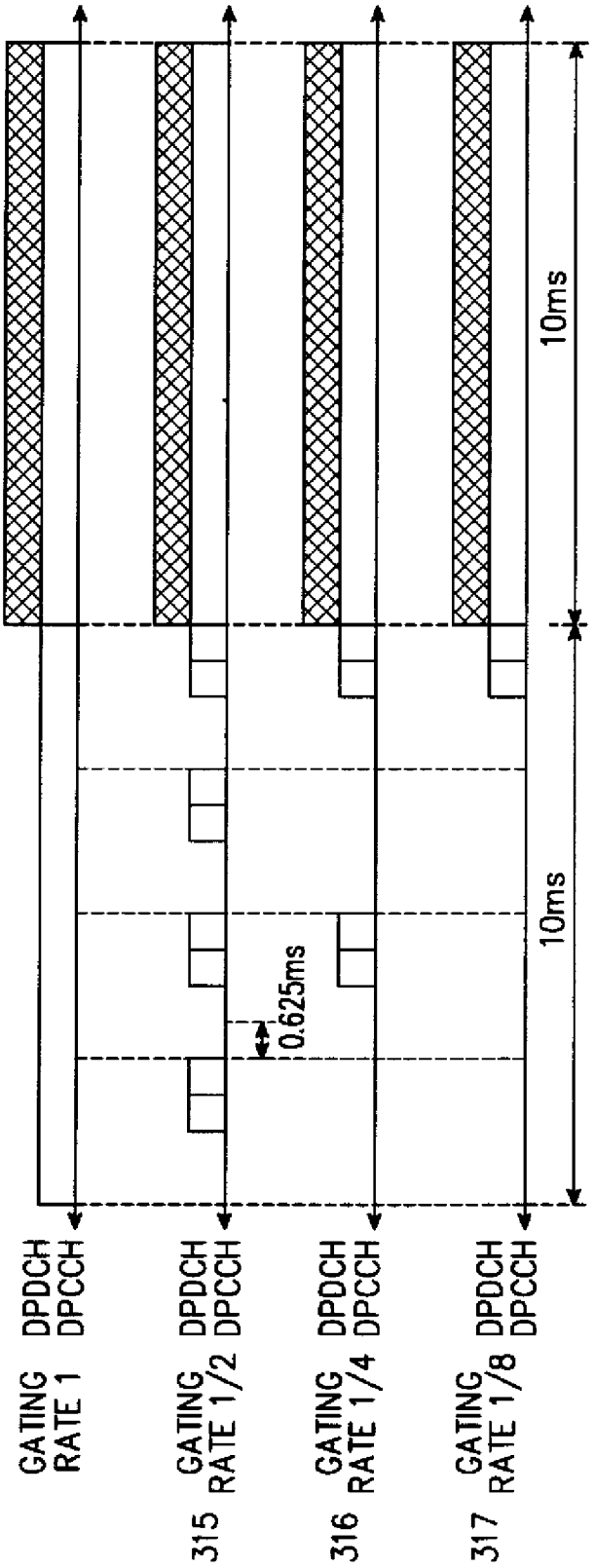

GATING RATE 1
DPDCH
DPCCH
315
GATING RATE 1/2
DPDCH
DPCCH
316
GATING RATE 1/4
DPDCH
DPCCH
317
GATING RATE 1/8
DPDCH
DPCCH
0.625ms
10ms
10ms

FIG. 8A

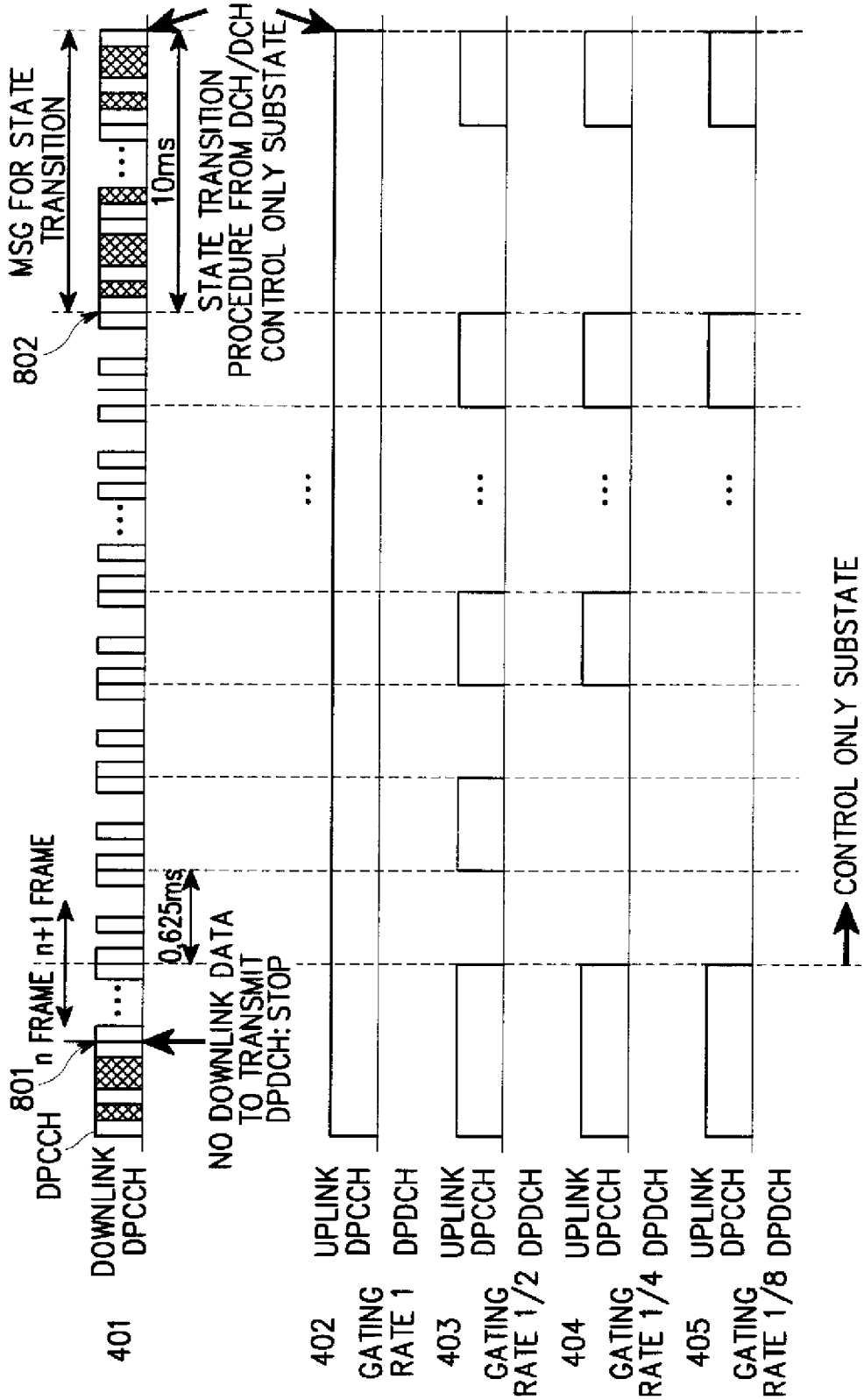

401
DOWNLINK DPCCH
DPCCH
801
n FRAME
n+1 FRAME
0.625ms
NO DOWNLINK DATA TO TRANSMIT DPDCH: STOP
802
MSG FOR STATE TRANSITION
10ms
STATE TRANSITION PROCEDURE FROM DCH/DCH CONTROL ONLY SUBSTATE
CONTROL ONLY SUBSTATE
402
GATING RATE 1
UPLINK DPCCH
DPDCH
403
GATING RATE 1/2
UPLINK DPCCH
DPDCH
404
GATING RATE 1/4
UPLINK DPCCH
DPDCH
405
GATING RATE 1/8
UPLINK DPCCH
DPDCH

FIG. 8B

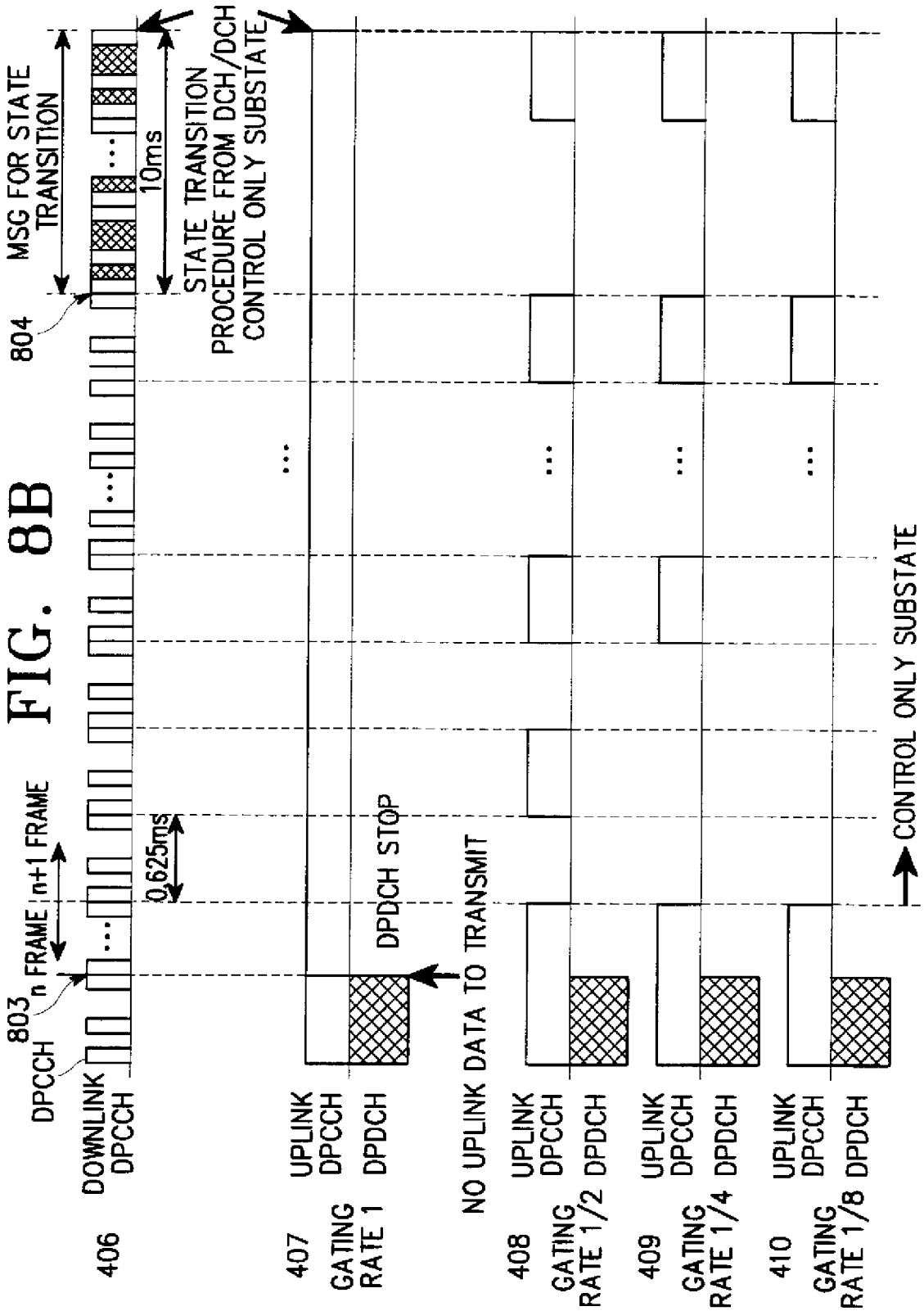

406
DOWNLINK DPCCH
DPCCH
803
n FRAME
n+1 FRAME
0.625ms
804
MSG FOR STATE TRANSITION
10ms
STATE TRANSITION PROCEDURE FROM DCH/DCH CONTROL ONLY SUBSTATE
407
GATING RATE 1
UPLINK DPCCH
DPDCH
DPDCH STOP
NO UPLINK DATA TO TRANSMIT
408
GATING RATE 1/2
UPLINK DPCCH
DPDCH
409
GATING RATE 1/4
UPLINK DPCCH
DPDCH
410
GATING RATE 1/8
UPLINK DPCCH
DPDCH
CONTROL ONLY SUBSTATE

FIG. 8C

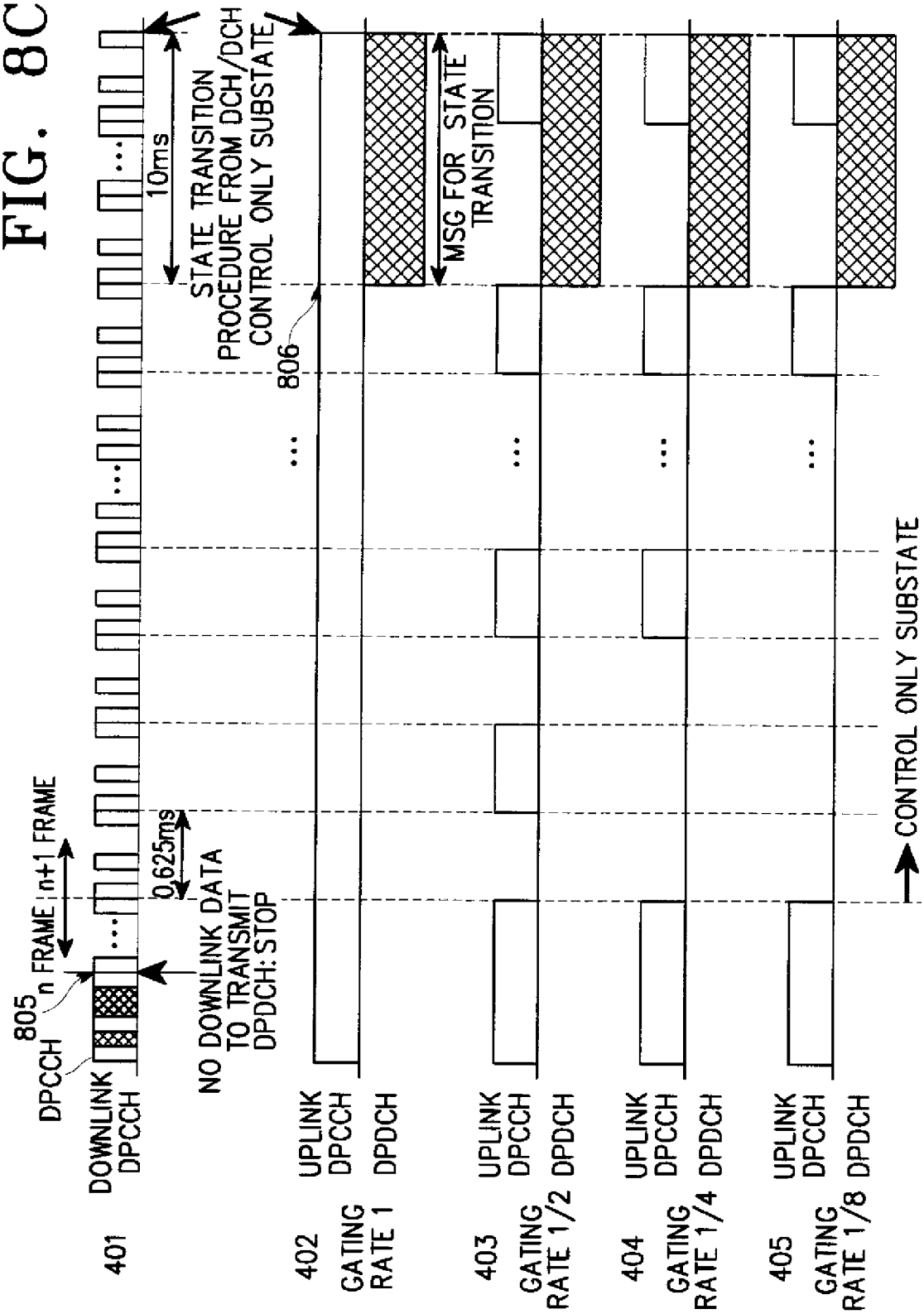

401
DOWNLINK DPCCH
DPCCH
805
n FRAME
n+1 FRAME
0.625ms
NO DOWNLINK DATA TO TRANSMIT DPDCH: STOP
10ms
STATE TRANSITION PROCEDURE FROM DCH/DCH CONTROL ONLY SUBSTATE
806
MSG FOR STATE TRANSITION
402
UPLINK DPCCH
GATING RATE 1
DPDCH
403
UPLINK DPCCH
GATING RATE 1/2
DPDCH
404
UPLINK DPCCH
GATING RATE 1/4
DPDCH
405
UPLINK DPCCH
GATING RATE 1/8
DPDCH
CONTROL ONLY SUBSTATE

FIG. 8D

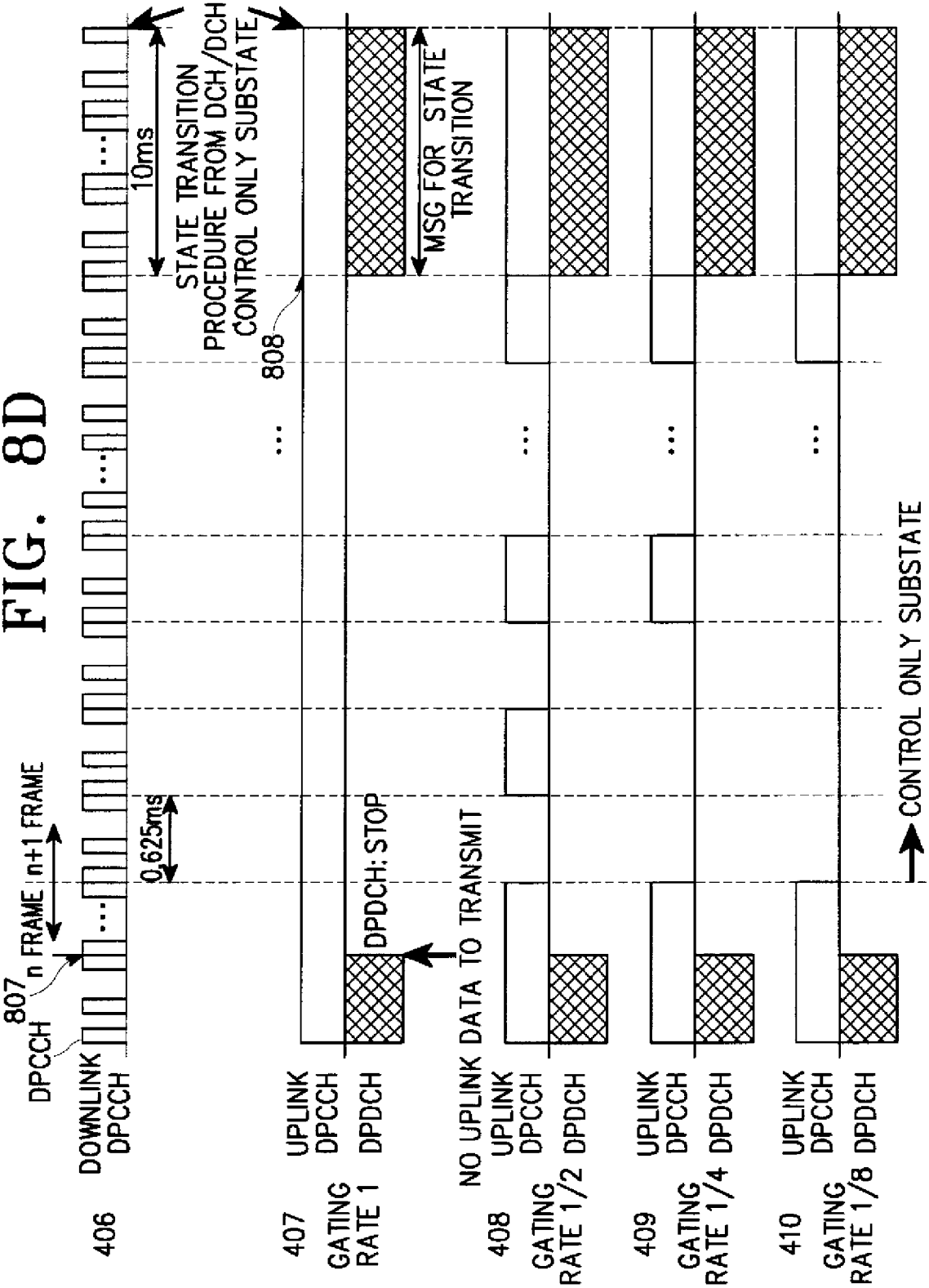

406
DOWNLINK DPCCH
DPCCH
807
n FRAME
n+1 FRAME
0.625ms
10ms
STATE TRANSITION PROCEDURE FROM DCH/DCH CONTROL ONLY SUBSTATE
808
MSG FOR STATE TRANSITION
407
GATING RATE 1
UPLINK DPCCH
DPDCH
DPDCH: STOP
NO UPLINK DATA TO TRANSMIT
408
GATING RATE 1/2
UPLINK DPCCH
DPDCH
409
GATING RATE 1/4
UPLINK DPCCH
DPDCH
410
GATING RATE 1/8
UPLINK DPCCH
DPDCH
CONTROL ONLY SUBSTATE

FIG. 9A

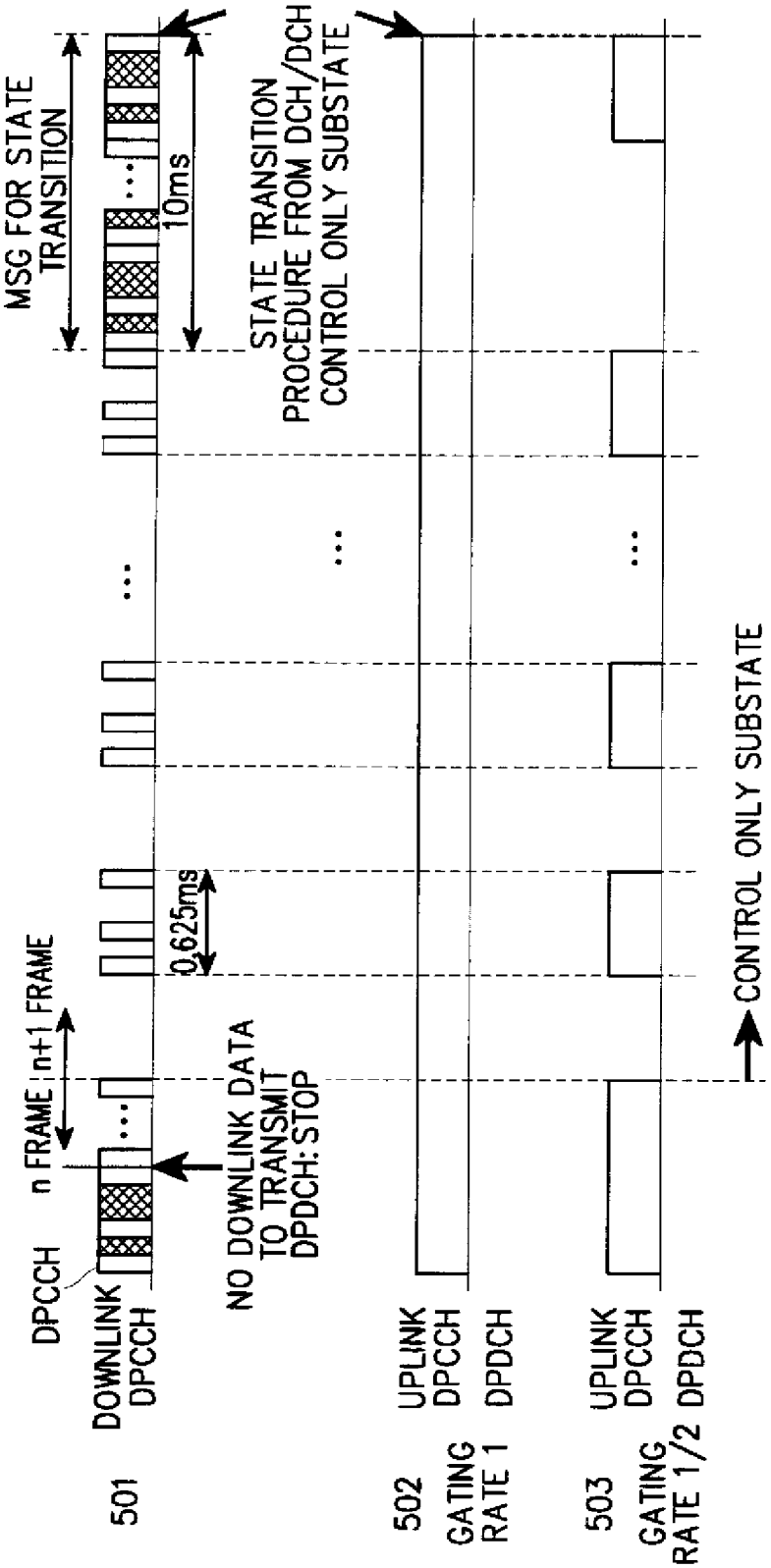

MSG FOR STATE TRANSITION
10ms
STATE TRANSITION PROCEDURE FROM DCH/DCH CONTROL ONLY SUBSTATE
n FRAME
n+1 FRAME
0.625ms
DPCCH
DOWNLINK DPCCH
NO DOWNLINK DATA TO TRANSMIT DPDCH: STOP
CONTROL ONLY SUBSTATE
501
502
GATING RATE 1
UPLINK DPCCH
DPDCH
503
GATING RATE 1/2
UPLINK DPCCH
DPDCH

FIG. 9B

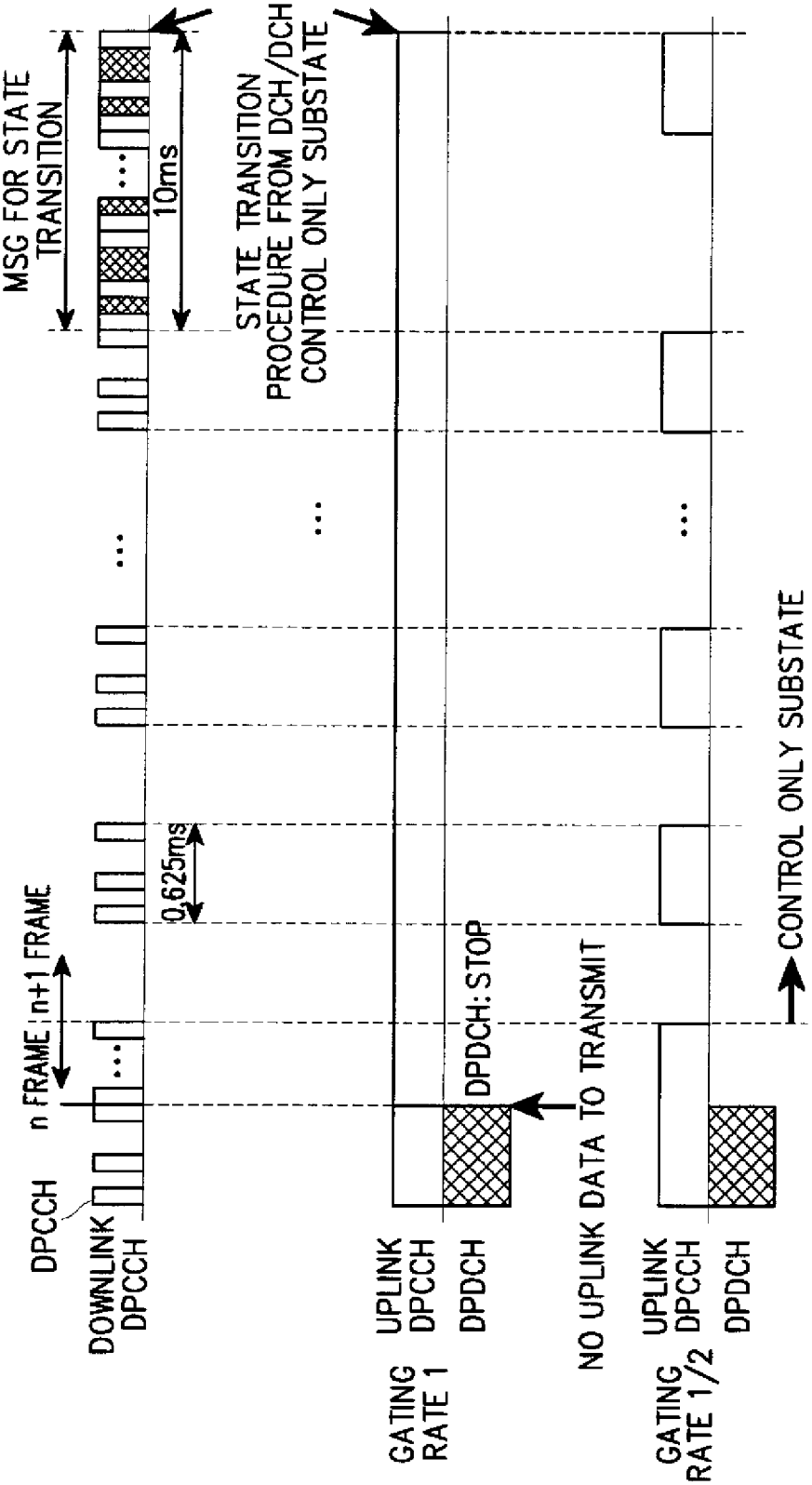

MSG FOR STATE TRANSITION
10ms
STATE TRANSITION PROCEDURE FROM DCH/DCH CONTROL ONLY SUBSTATE
n FRAME
n+1 FRAME
0.625ms
DPCCH
DOWNLINK DPCCH
UPLINK DPCCH
DPDCH
DPDCH: STOP
NO UPLINK DATA TO TRANSMIT
CONTROL ONLY SUBSTATE
GATING RATE 1
GATING RATE 1/2

FIG. 10A

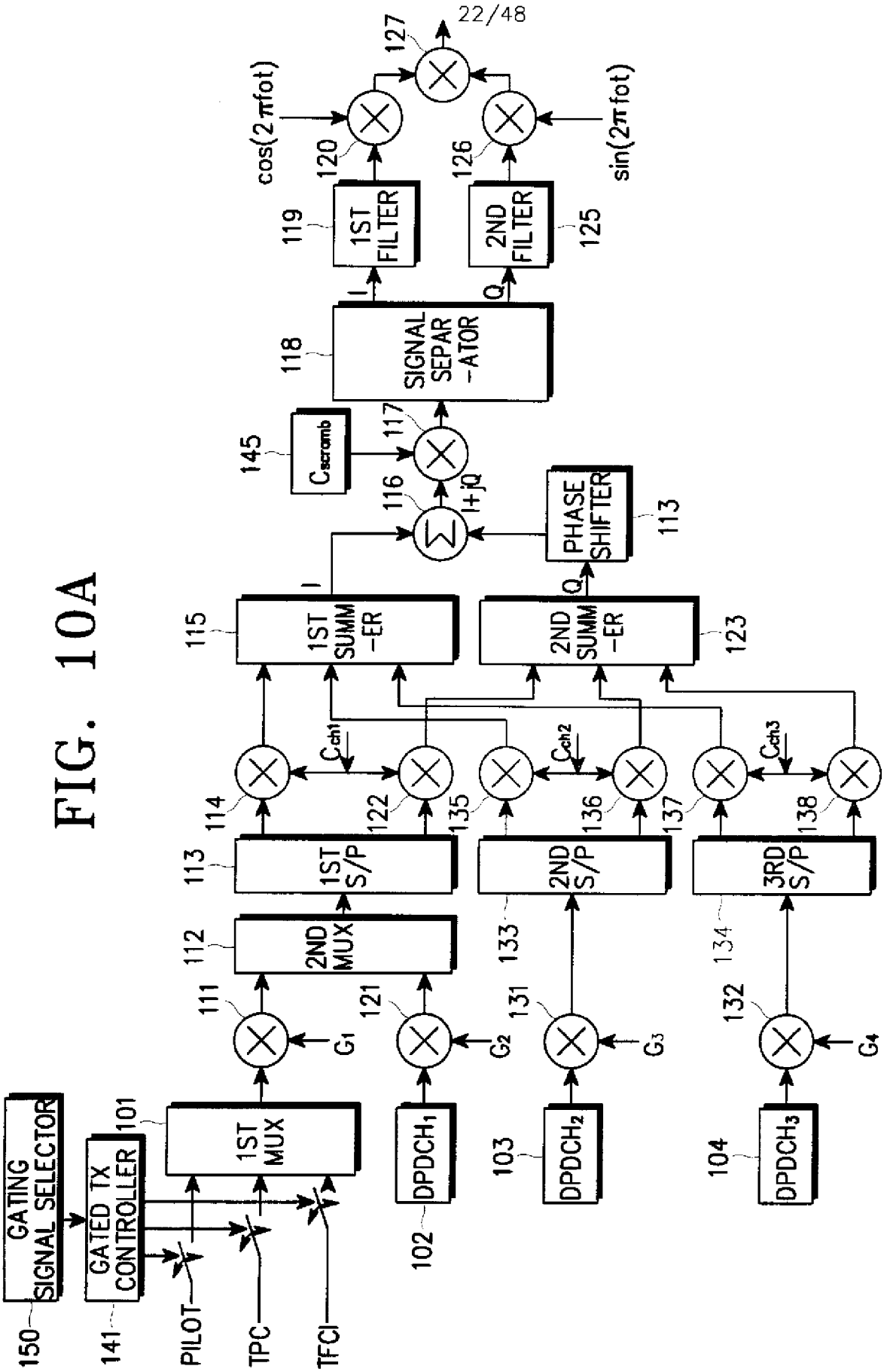
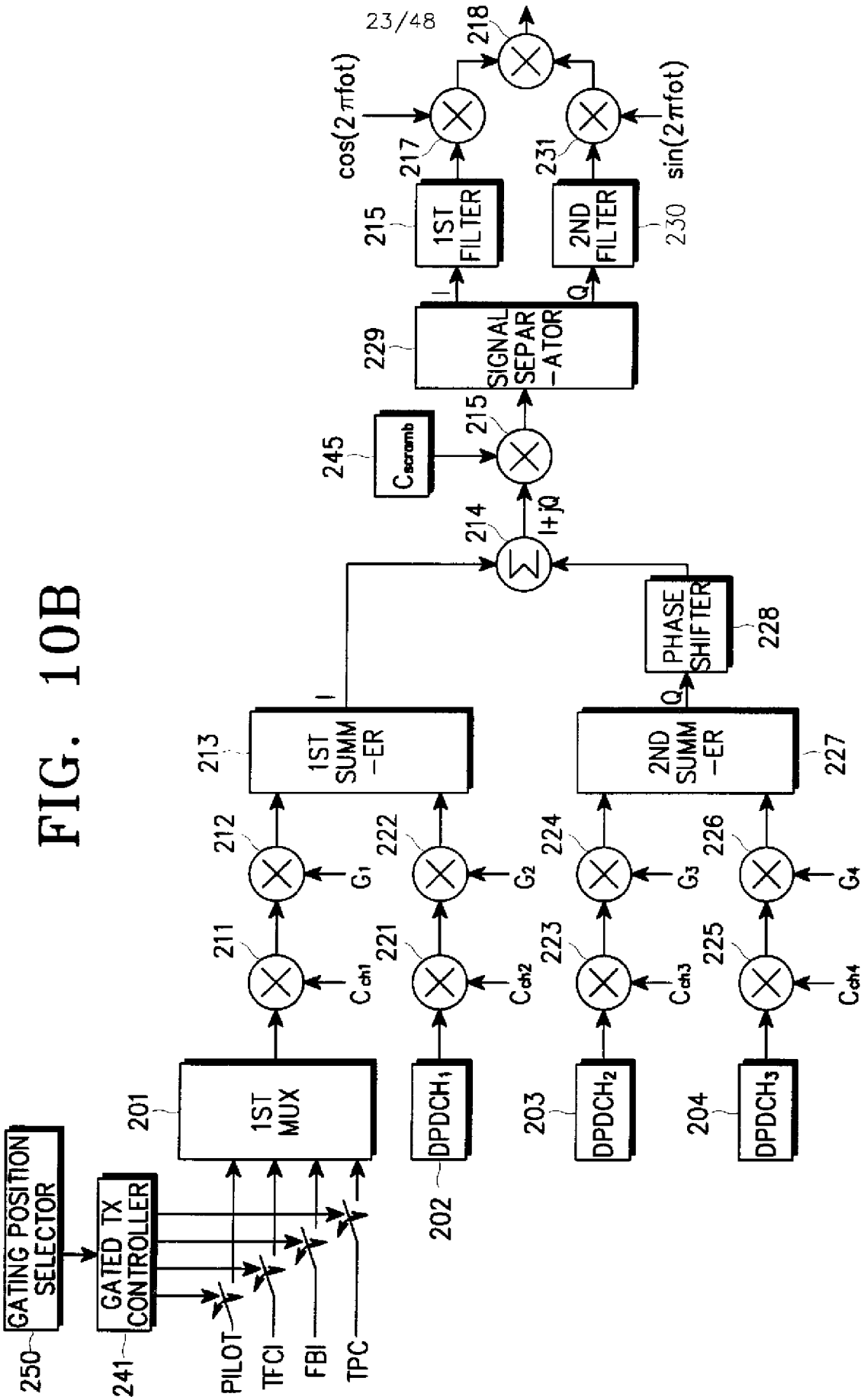

GATING SIGNAL SELECTOR
150
GATED TX CONTROLLER
141
101
1ST MUX
PILOT
TPC
TFCI
DPDCH1
102
DPDCH2
103
DPDCH3
104
G1
G2
G3
G4
111
121
131
132
2ND MUX
112
1ST S/P
113
2ND S/P
133
3RD S/P
134
114
122
135
136
137
138
Cch1
Cch2
Cch3
1ST SUMM -ER
115
2ND SUMM -ER
123
I
Q
PHASE SHIFTER
113
1+jQ
116
Cscramb
145
117
SIGNAL SEPAR -ATOR
118
1ST FILTER
119
2ND FILTER
125
cos(2πfot)
sin(2πfot)
120
126
127

FIG. 10B


GATING POSITION SELECTOR
250
GATED TX CONTROLLER
241
PILOT
TFCI
FBI
TPC
1ST MUX
201
DPDCH1
202
DPDCH2
203
DPDCH3
204
Cch1
Cch2
Cch3
Cch4
G1
G2
G3
G4
211
212
221
222
223
224
225
226
1ST SUMM -ER
213
2ND SUMM -ER
227
PHASE SHIFTER
228
I
Q
214
I+jQ
215
Cscramb
245
SIGNAL SEPAR -ATOR
229
1ST FILTER
215
2ND FILTER
230
217
231
cos(2πfot)
sin(2πfot)
218

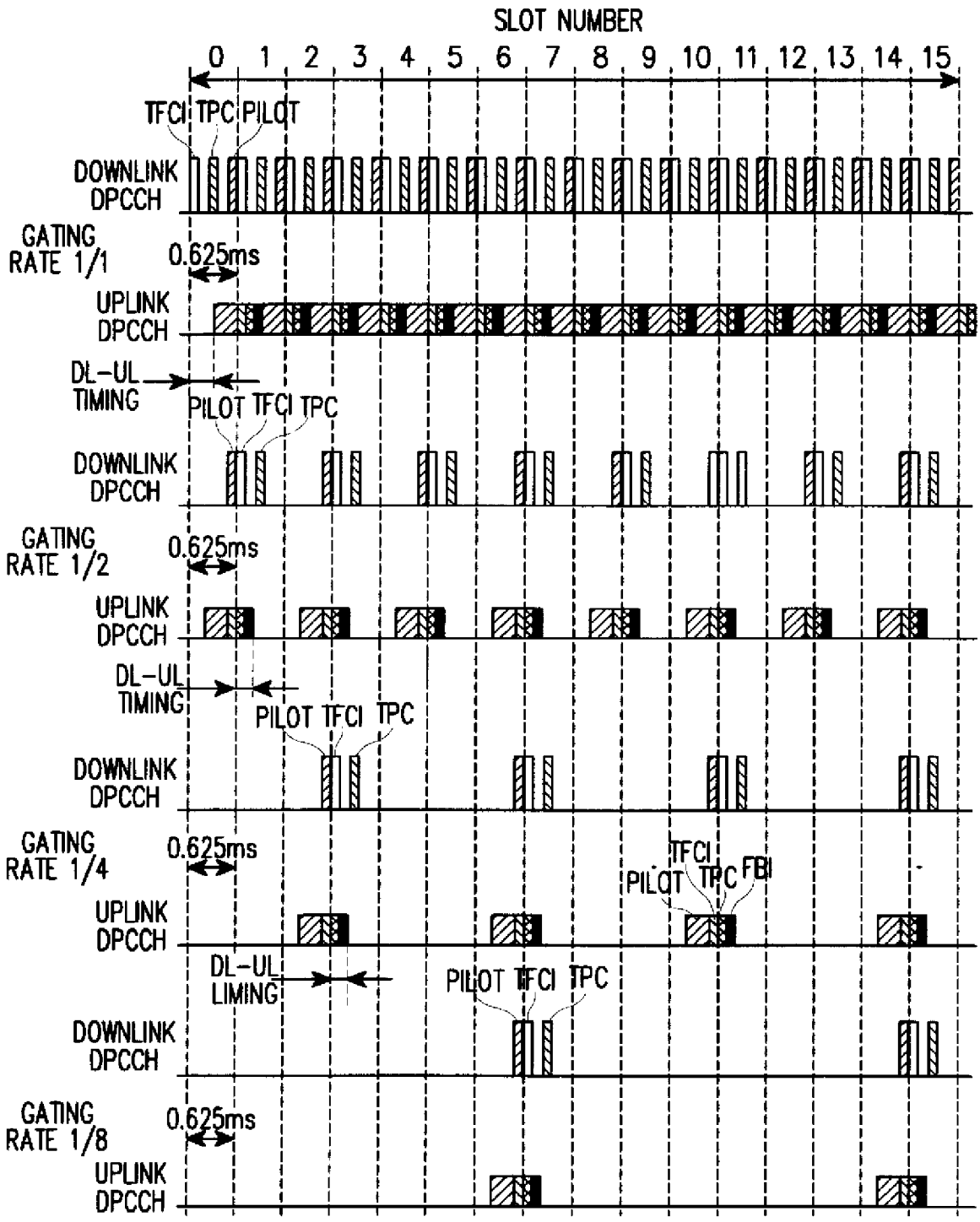

SLOT NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
TFCI TPC PILOT
DOWNLINK DPCCH
GATING RATE 1/1
0.625ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/2
0.625ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/4
0.625ms
TFCI
PILOT TPC FBI
UPLINK DPCCH
DL-UL LIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/8
0.625ms
UPLINK DPCCH

FIG. 11A

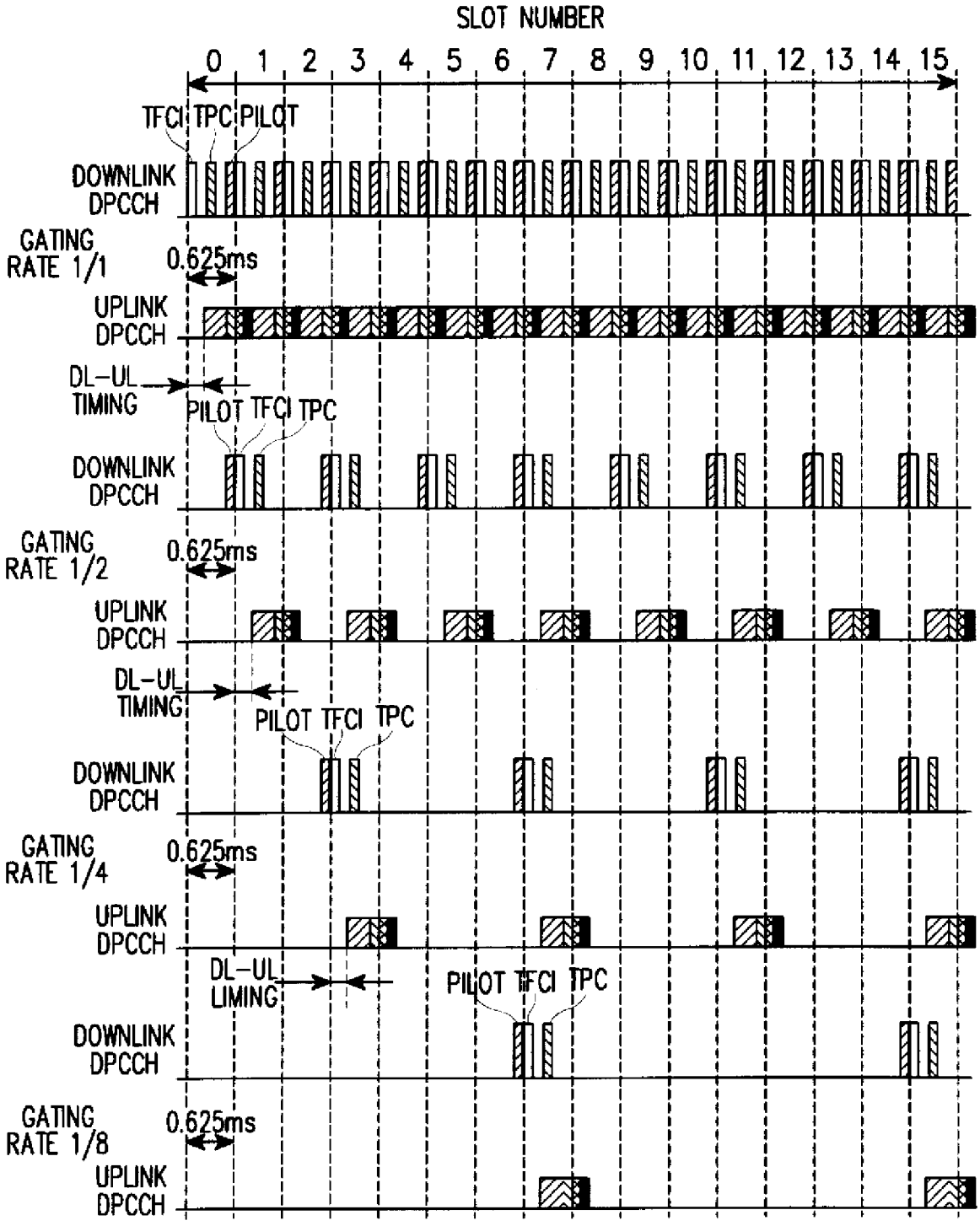

SLOT NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
TFCI TPC PILOT
DOWNLINK DPCCH
GATING RATE 1/1
0.625ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/2
0.625ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/4
0.625ms
UPLINK DPCCH
DL-UL LIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/8
0.625ms
UPLINK DPCCH

FIG. 11B

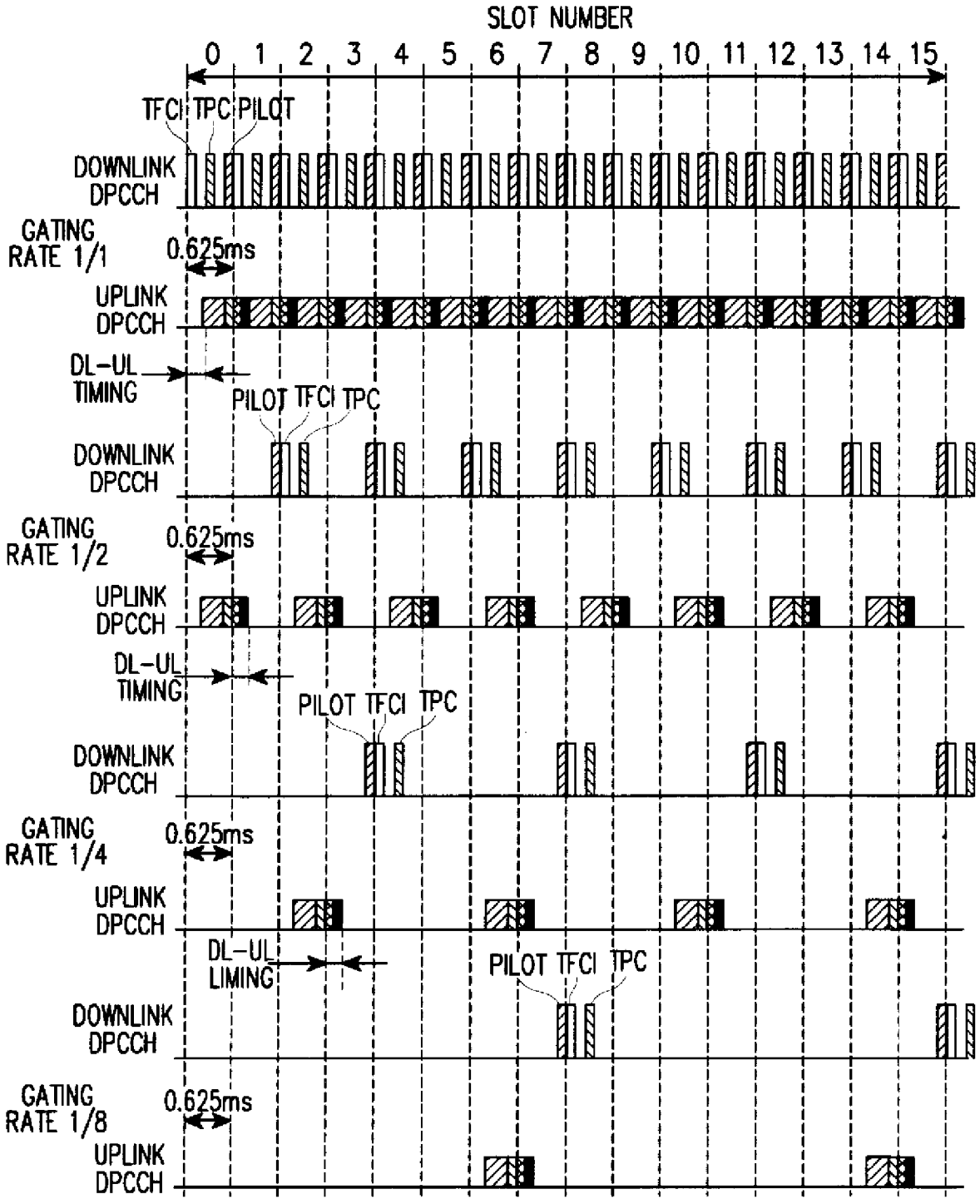

SLOT NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
TFCI TPC PILOT
DOWNLINK DPCCH
GATING RATE 1/1
0.625ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/2
0.625ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/4
0.625ms
UPLINK DPCCH
DL-UL LIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/8
0.625ms
UPLINK DPCCH

FIG. 11C

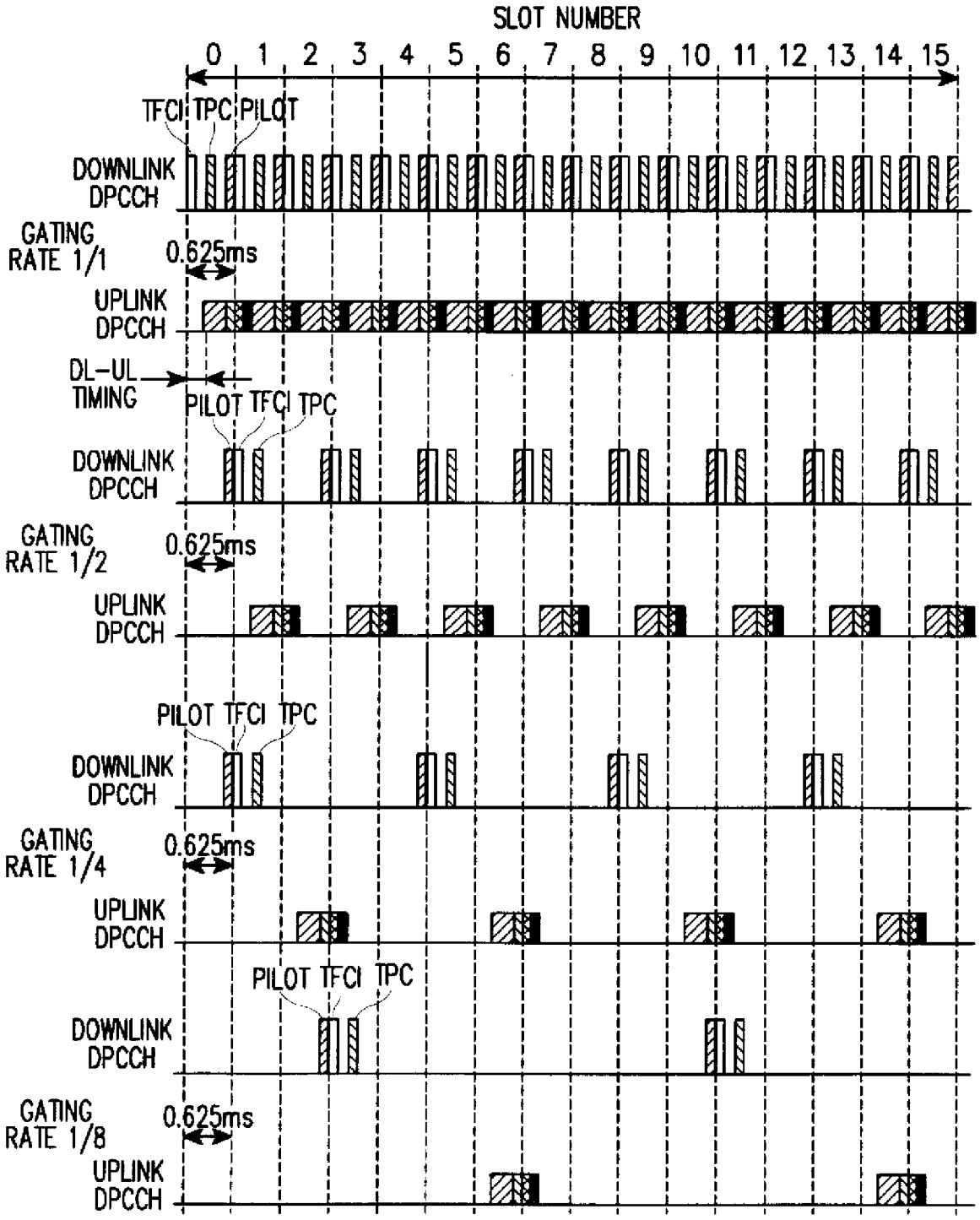

SLOT NUMBER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
TFCI TPC PILOT
DOWNLINK DPCCH
GATING RATE 1/1
0.625ms
UPLINK DPCCH
DL-UL TIMING
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/2
0.625ms
UPLINK DPCCH
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/4
0.625ms
UPLINK DPCCH
PILOT TFCI TPC
DOWNLINK DPCCH
GATING RATE 1/8
0.625ms
UPLINK DPCCH

FIG. 11D

FIG. 12A

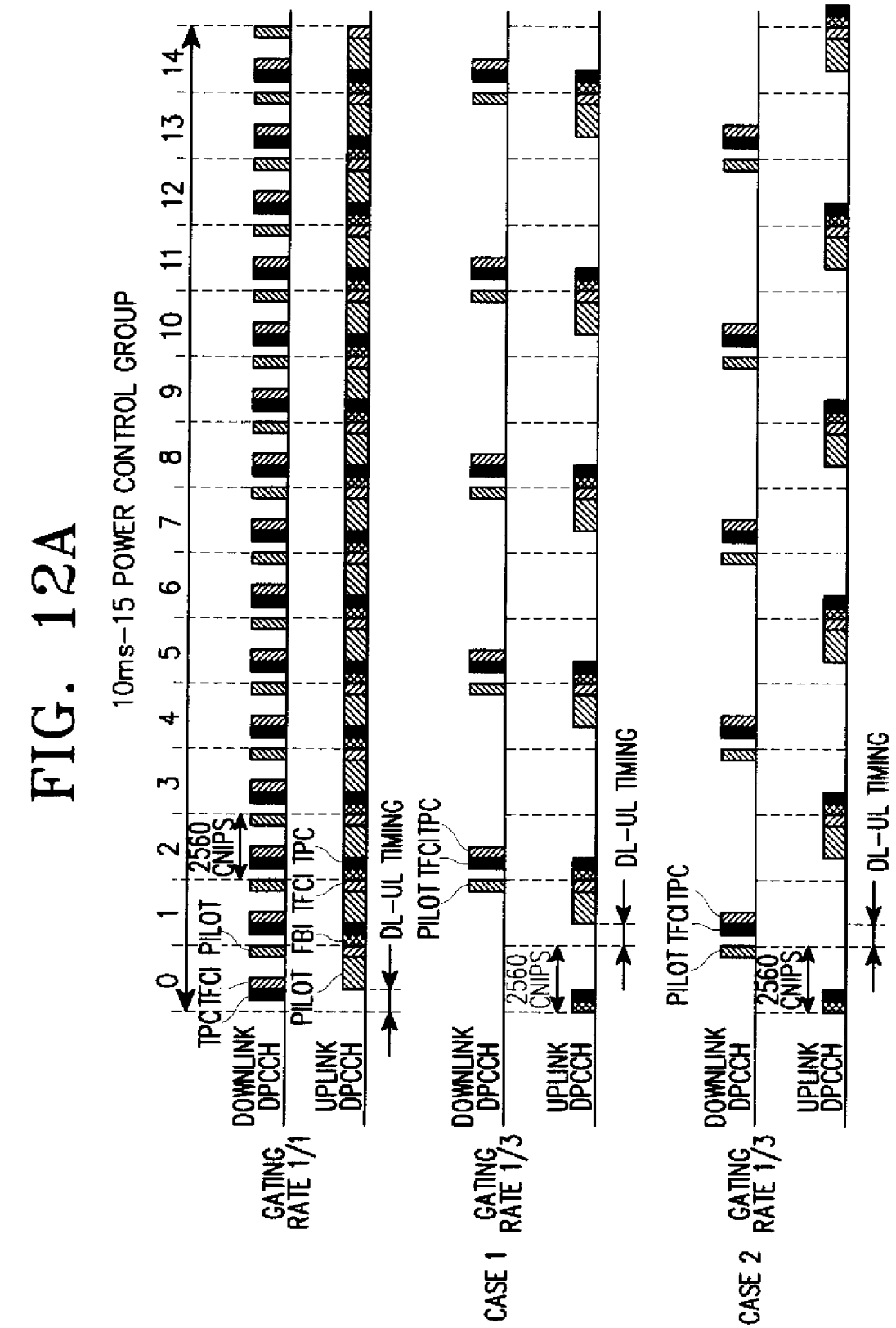

10ms-15 POWER CONTROL GROUP
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
2560 CNIPS
TPC TFCI PILOT
PILOT FBI TFCI TPC
DL-UL TIMING
DOWNLINK DPCCH
UPLINK DPCCH
GATING RATE 1/1
PILOT TFCI TPC
CASE 1
GATING RATE 1/3
CASE 2

FIG. 12B

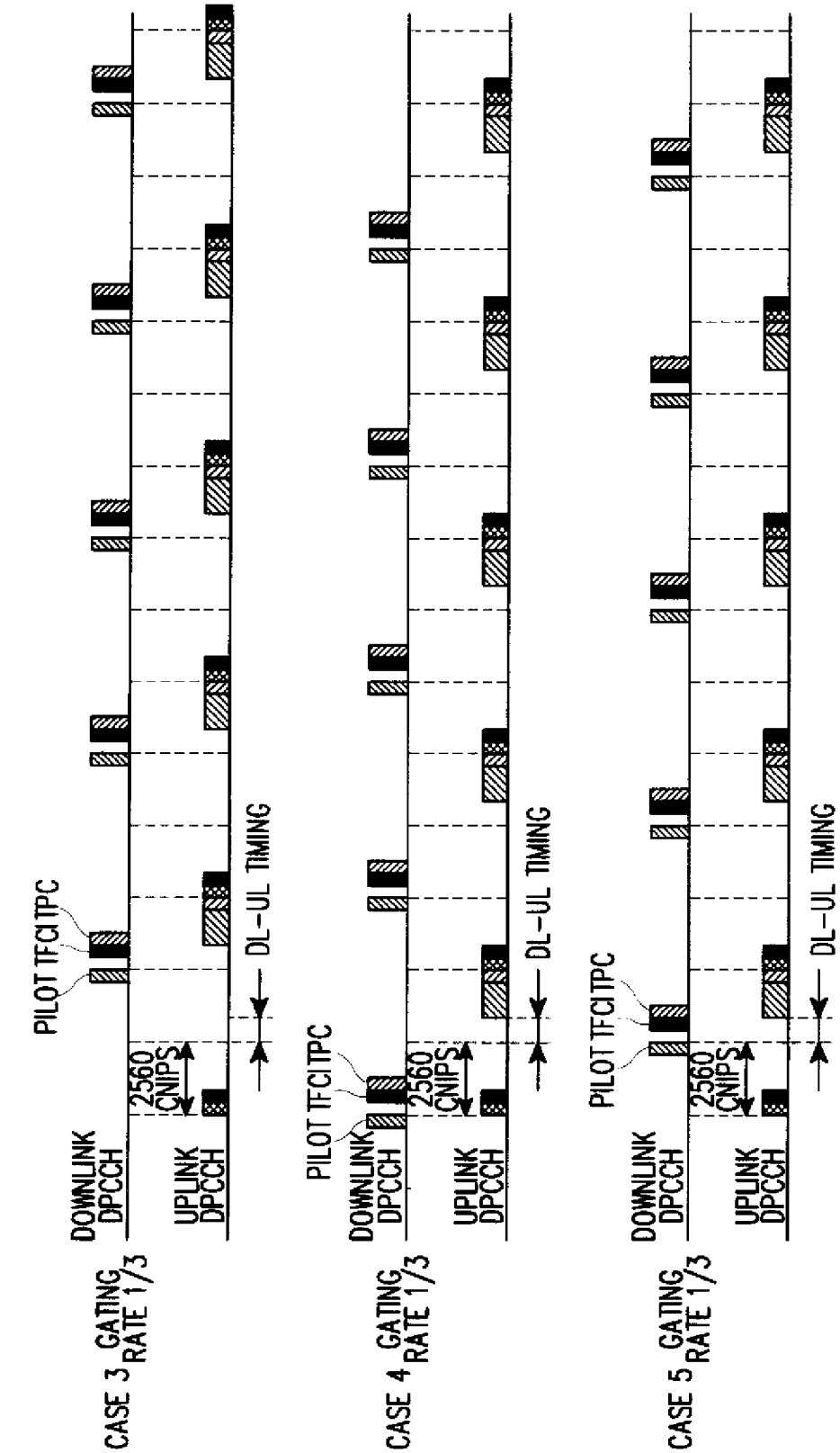

10ms-15POWER CONTROL GROUP
CASE 3 GATING RATE 1/3
CASE 4 GATING RATE 1/3
CASE 5 GATING RATE 1/3
PILOT TFCI TPC
DOWNLINK DPCCH
UPLINK DPCCH
2560 CNIPS
DL-UL TIMING

FIG. 12C

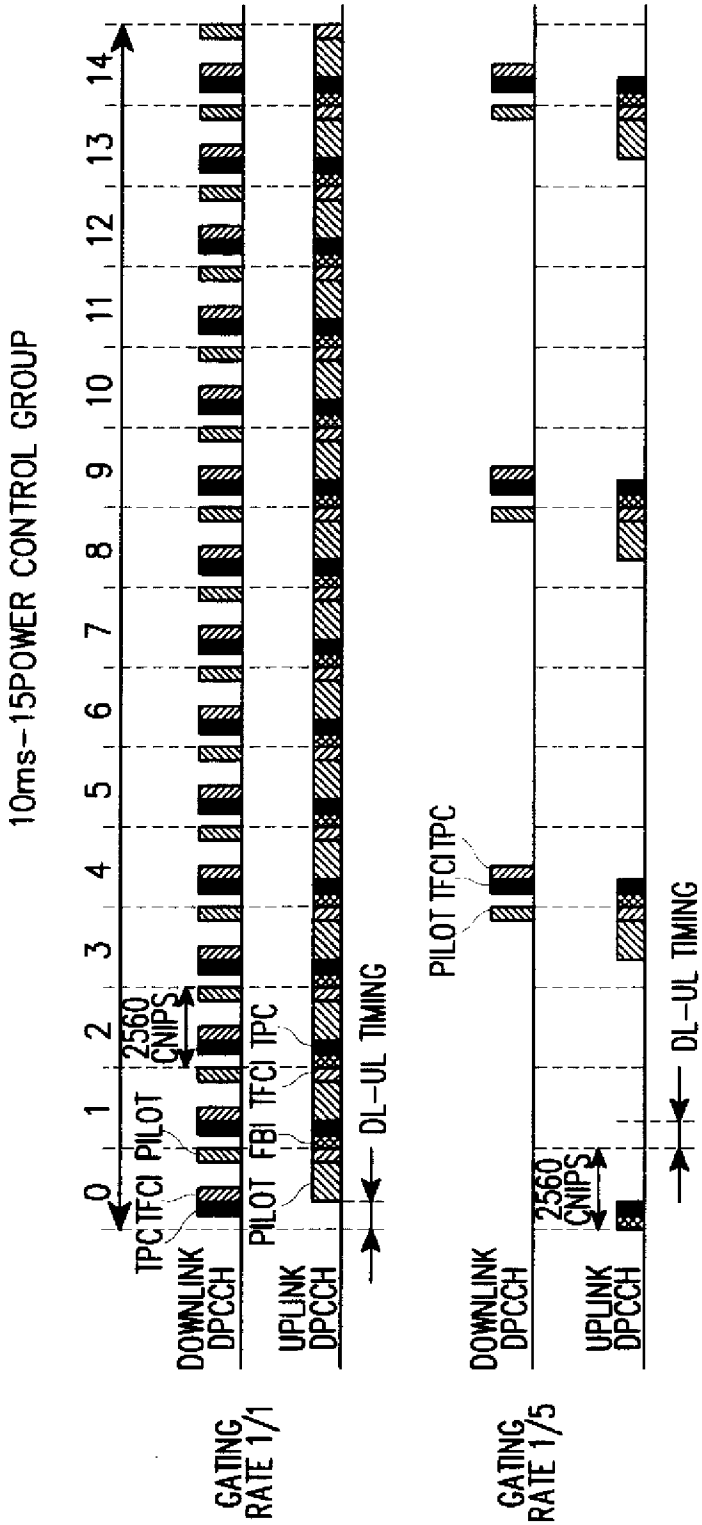

10ms-15POWER CONTROL GROUP
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
2560 CNIPS
TPC TFCI PILOT
PILOT FBI TFCI TPC
DOWNLINK DPCCH
UPLINK DPCCH
DL-UL TIMING
GATING RATE 1/1
PILOT TFCI TPC
2560 CNIPS
DOWNLINK DPCCH
UPLINK DPCCH
DL-UL TIMING
GATING RATE 1/5

FIG. 12D

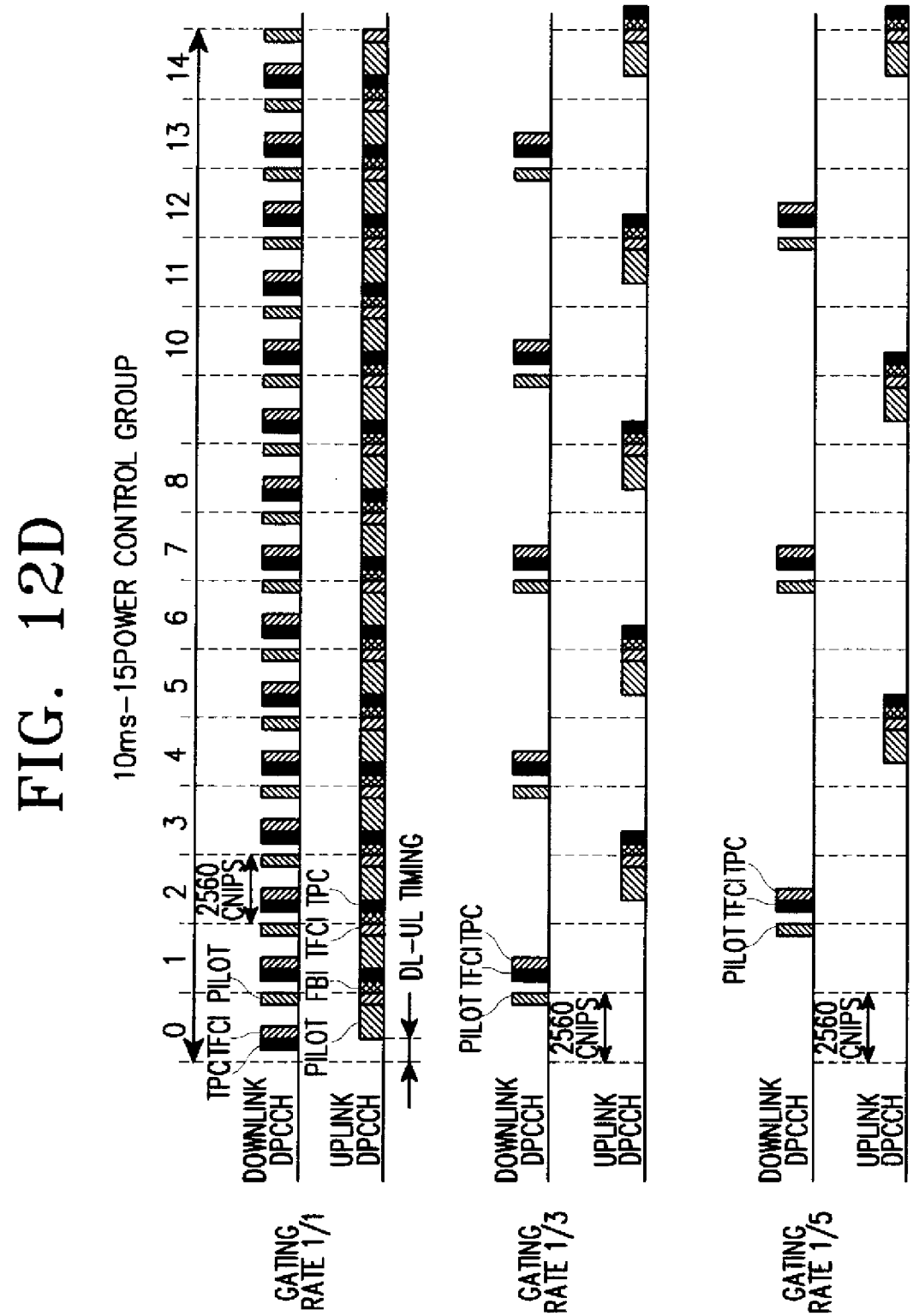

10ms-15POWER CONTROL GROUP
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
2560 CNIPS
TPC TFCI PILOT
PILOT FBI TFCI TPC
DL-UL TIMING
DOWNLINK DPCCH
UPLINK DPCCH
GATING RATE 1/1
PILOT TFCI TPC
2560 CNIPS
DOWNLINK DPCCH
UPLINK DPCCH
GATING RATE 1/3
PILOT TFCI TPC
2560 CNIPS
DOWNLINK DPCCH
UPLINK DPCCH
GATING RATE 1/5

FIG. 12E

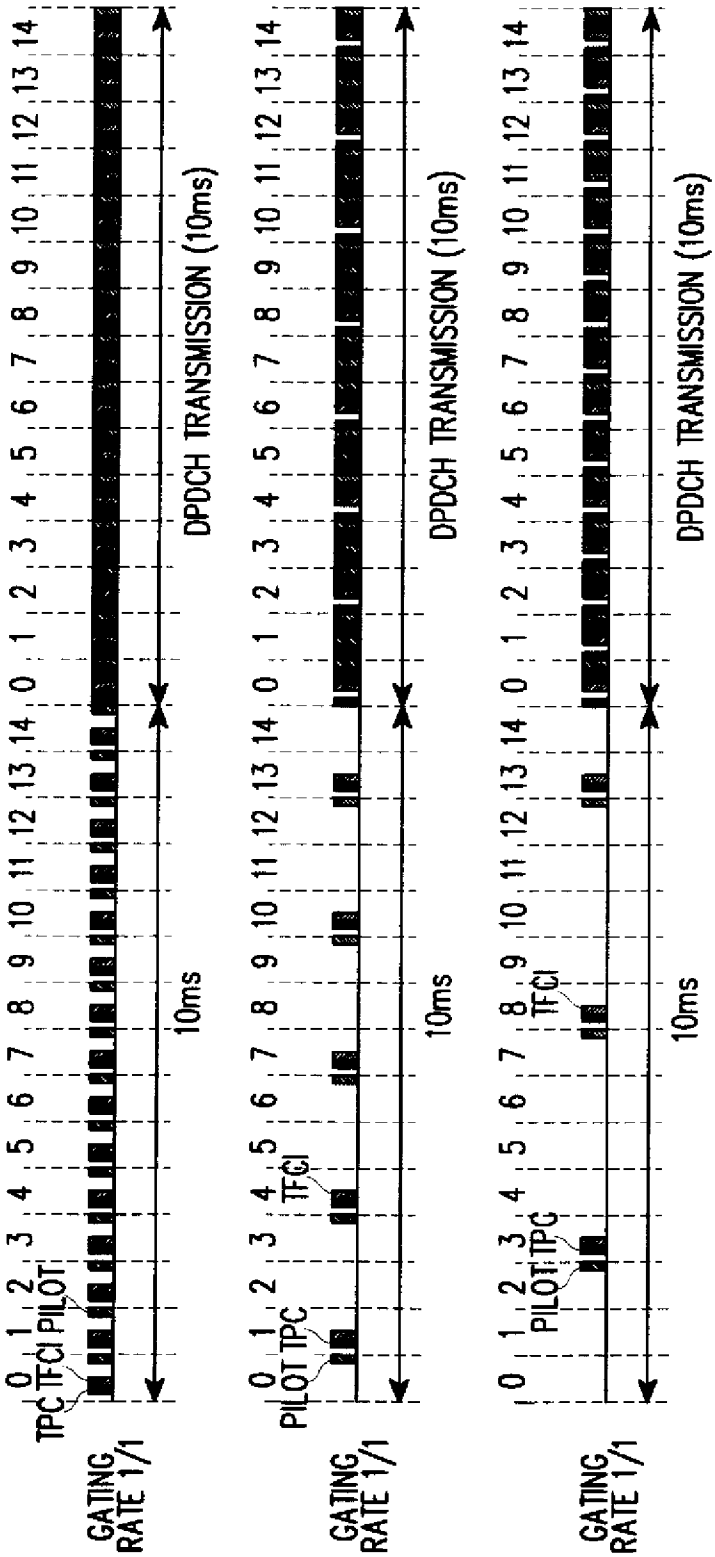

GATING RATE 1/1
TPC TFCI PILOT
DPDCH TRANSMISSION (10ms)
10ms
GATING RATE 1/1
PILOT TPC TFCI
DPDCH TRANSMISSION (10ms)
10ms
GATING RATE 1/1
PILOT TPC TFCI
DPDCH TRANSMISSION (10ms)
10ms

FIG. 13A

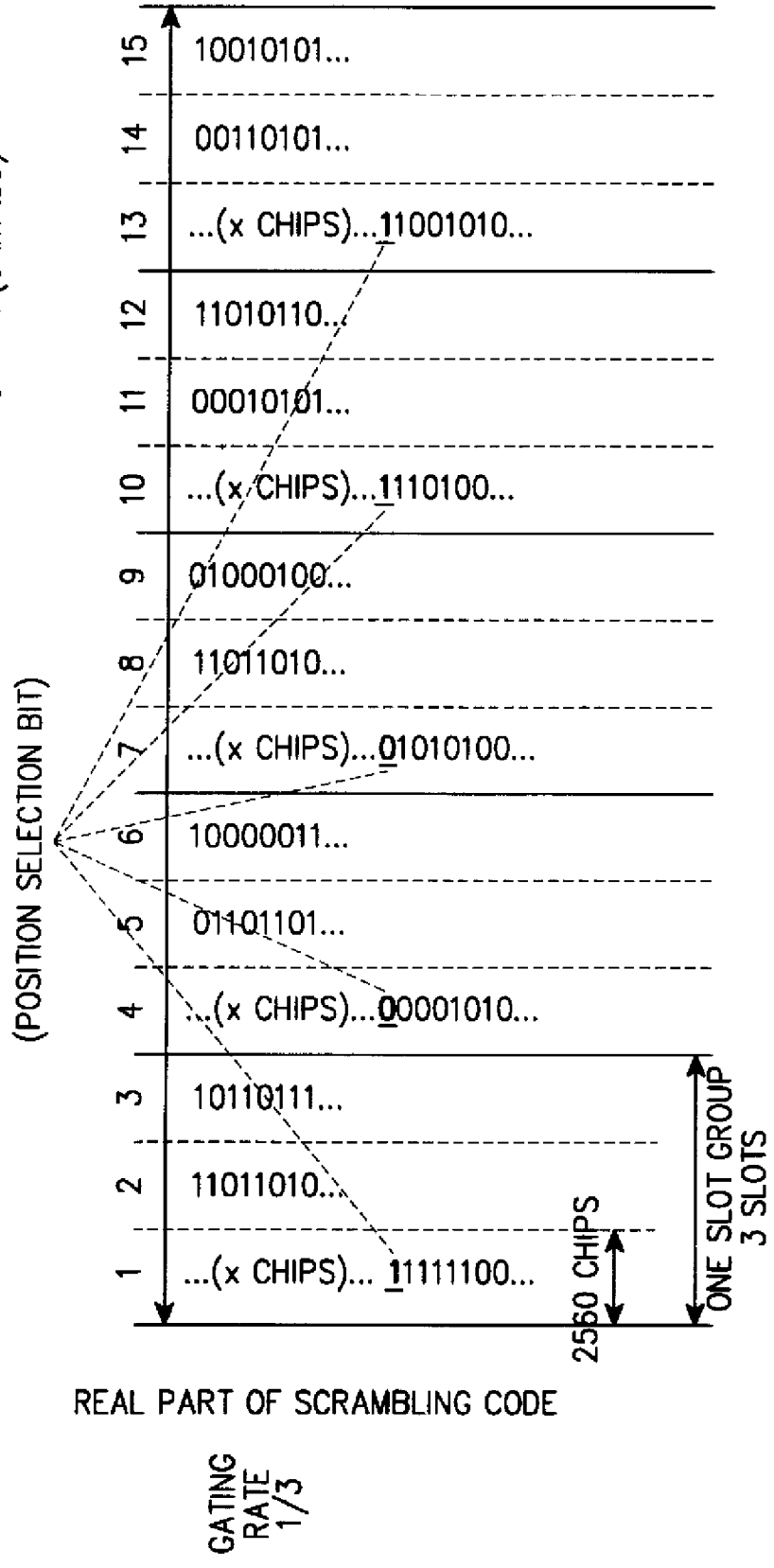

10ms=15 POWER CONTROL GROUP
x = SFN*m (0<m<36)
(POSITION SELECTION BIT)
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
10010101...
00110101...
...(x CHIPS)...11001010...
11010110...
00010101...
...(x CHIPS)...1110100...
01000100...
11011010...
...(x CHIPS)...01010100...
10000011...
01101101...
...(x CHIPS)...00001010...
10110111...
11011010...
...(x CHIPS)... 11111100...
2560 CHIPS
ONE SLOT GROUP
3 SLOTS
REAL PART OF SCRAMBLING CODE
GATING
RATE
1/3

FIG. 13B

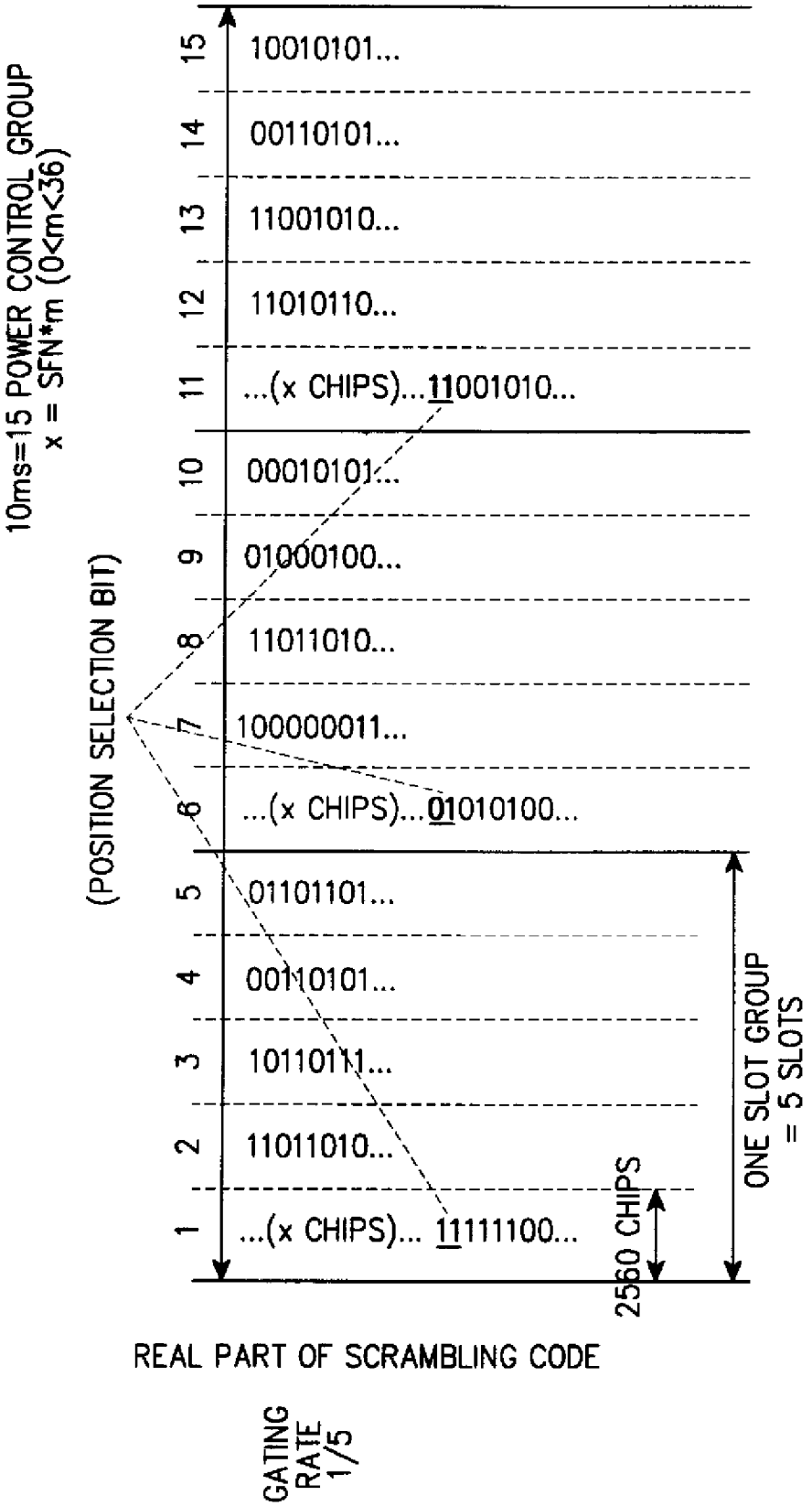

10ms=15 POWER CONTROL GROUP
x = SFN*m (0<m<36)
(POSITION SELECTION BIT)
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
10010101...
00110101...
11001010...
11010110...
...(x CHIPS)...11001010...
00010101...
01000100...
11011010...
100000011...
...(x CHIPS)...01010100...
01101101...
00110101...
10110111...
11011010...
...(x CHIPS)... 11111100...
2560 CHIPS
ONE SLOT GROUP
= 5 SLOTS
REAL PART OF SCRAMBLING CODE
GATING
RATE
1/5

FIG. 13C

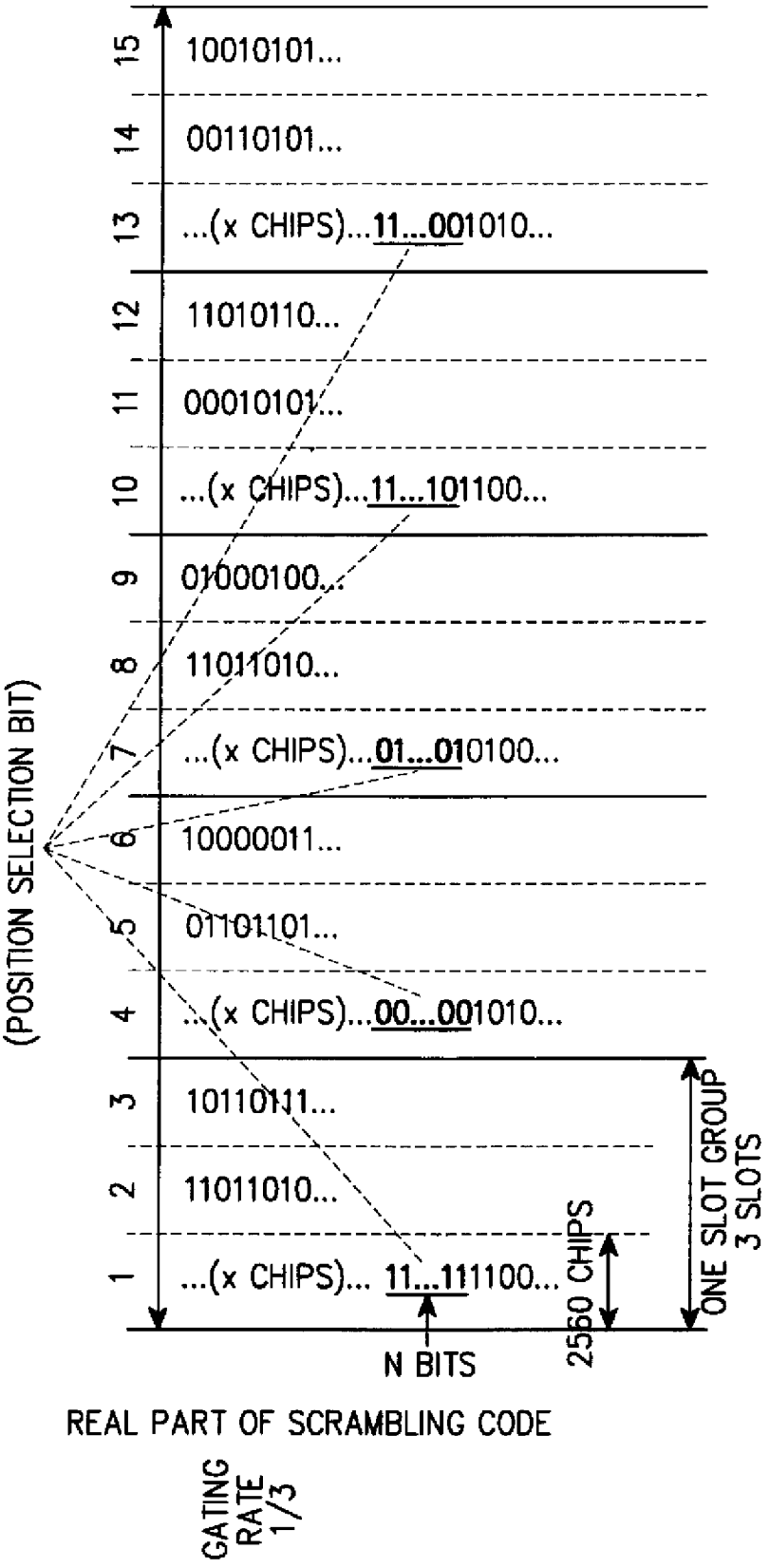

10ms=15 POWER CONTROL GROUP
x = SFN*m (0<m<36)
(POSITION SELECTION BIT)
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
10010101...
00110101...
...(x CHIPS)...11...001010...
11010110...
00010101...
...(x CHIPS)...11...101100...
01000100...
11011010...
...(x CHIPS)...01...010100...
10000011...
01101101...
...(x CHIPS)...00...001010...
10110111...
11011010...
...(x CHIPS)... 11...111100...
2560 CHIPS
ONE SLOT GROUP
3 SLOTS
N BITS
REAL PART OF SCRAMBLING CODE
GATING RATE 1/3

FIG. 13D

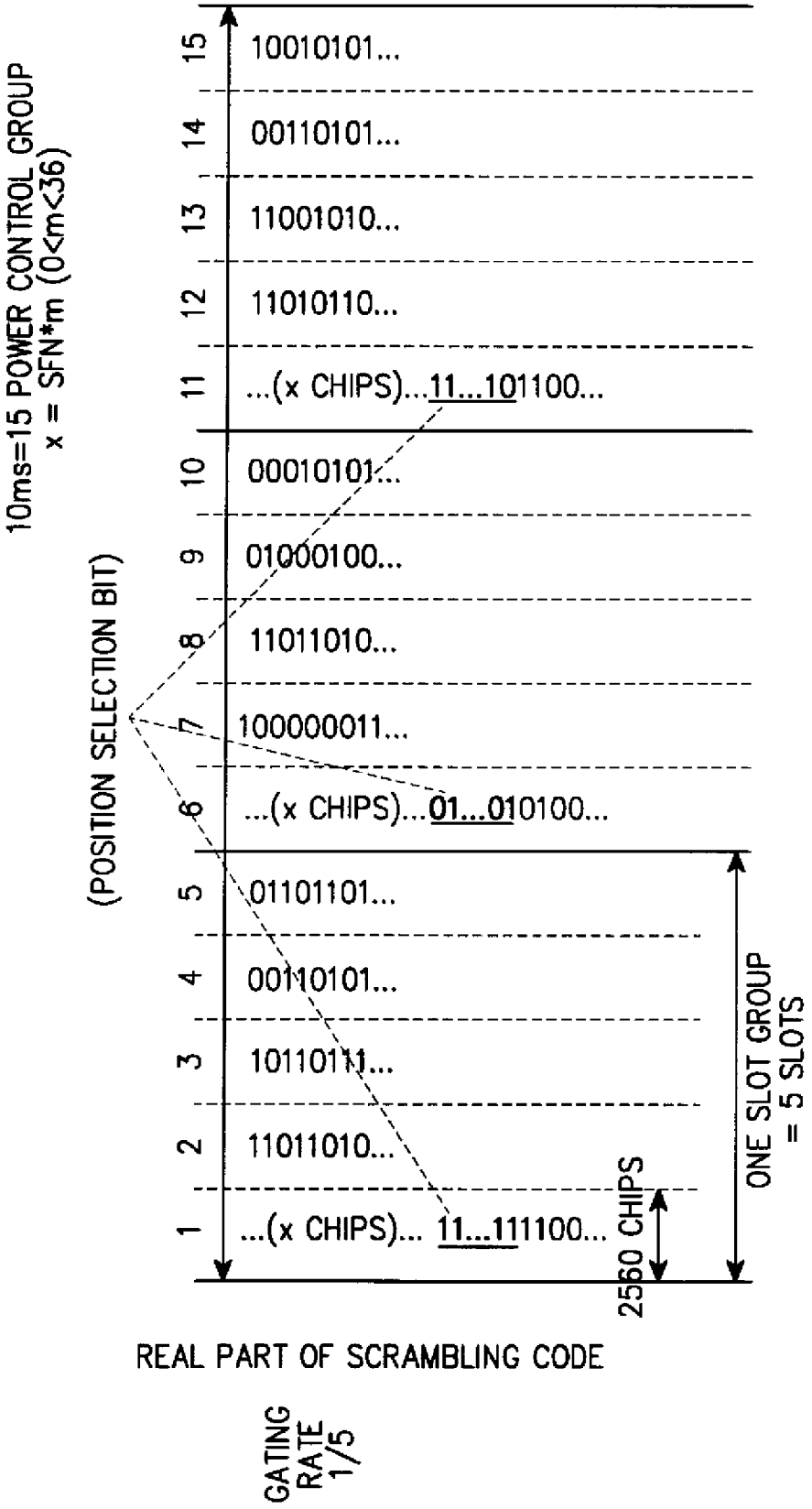

10ms=15 POWER CONTROL GROUP
x = SFN*m (0<m<36)
(POSITION SELECTION BIT)
15 10010101...
14 00110101...
13 11001010...
12 11010110...
11 ...(x CHIPS)...11...101100...
10 00010101...
9 01000100...
8 11011010...
7 100000011...
6 ...(x CHIPS)...01...010100...
5 01101101...
4 00110101...
3 10110111...
2 11011010...
1 ...(x CHIPS)... 11...111100...
2560 CHIPS
ONE SLOT GROUP
= 5 SLOTS
REAL PART OF SCRAMBLING CODE
GATING RATE 1/5

FIG. 14A

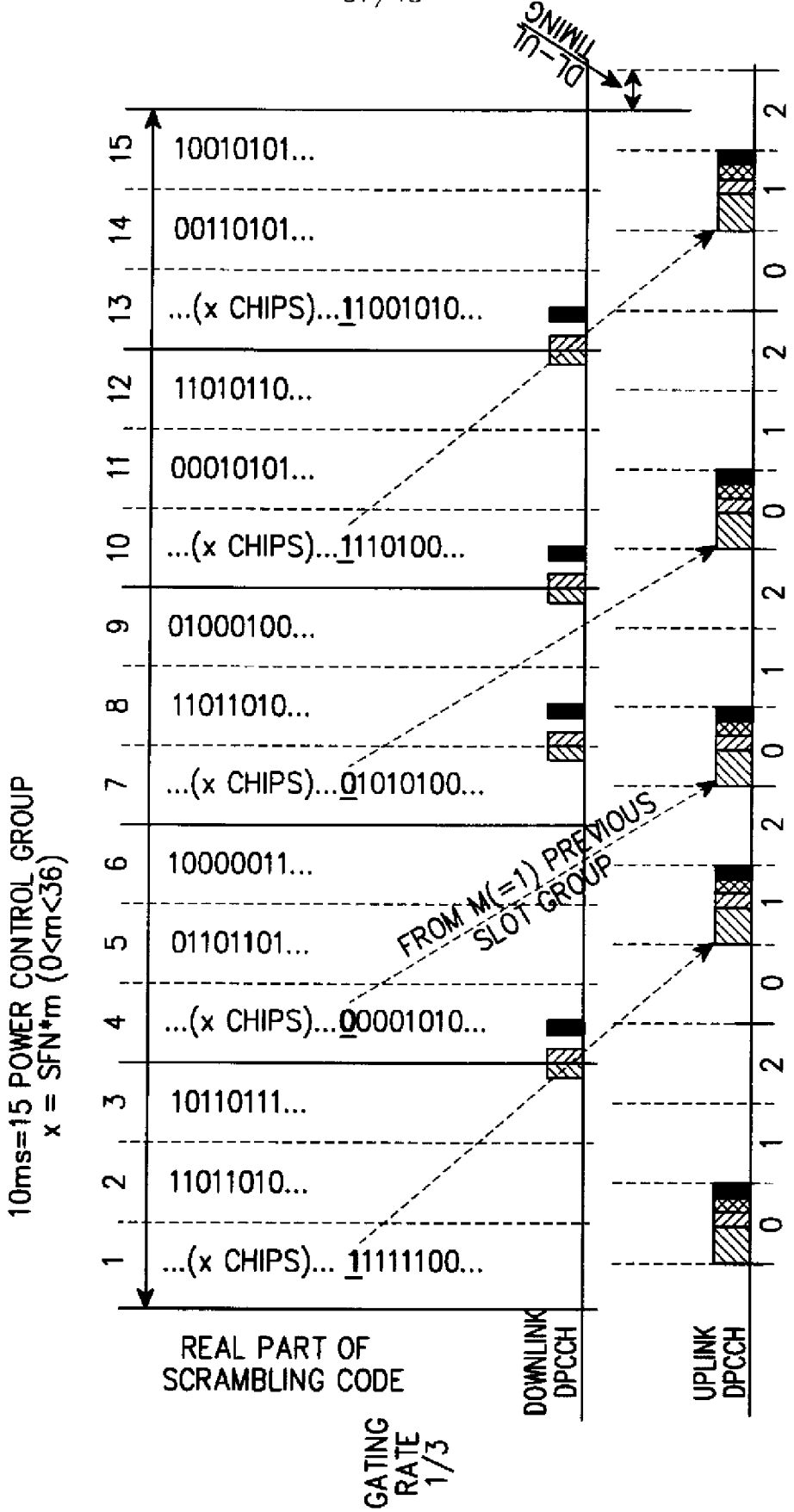

10ms=15 POWER CONTROL GROUP
x = SFN*m (0<m<36)
REAL PART OF SCRAMBLING CODE
GATING RATE 1/3
DOWNLINK DPCCH
UPLINK DPCCH
TIMING
FROM M(=1) PREVIOUS SLOT GROUP
10010101...
00110101...
...(x CHIPS)...11001010...
11010110...
00010101...
...(x CHIPS)...1110100...
01000100...
11011010...
...(x CHIPS)...01010100...
10000011...
01101101...
...(x CHIPS)...00001010...
10110111...
11011010...
...(x CHIPS)... 11111100...

FIG. 14B

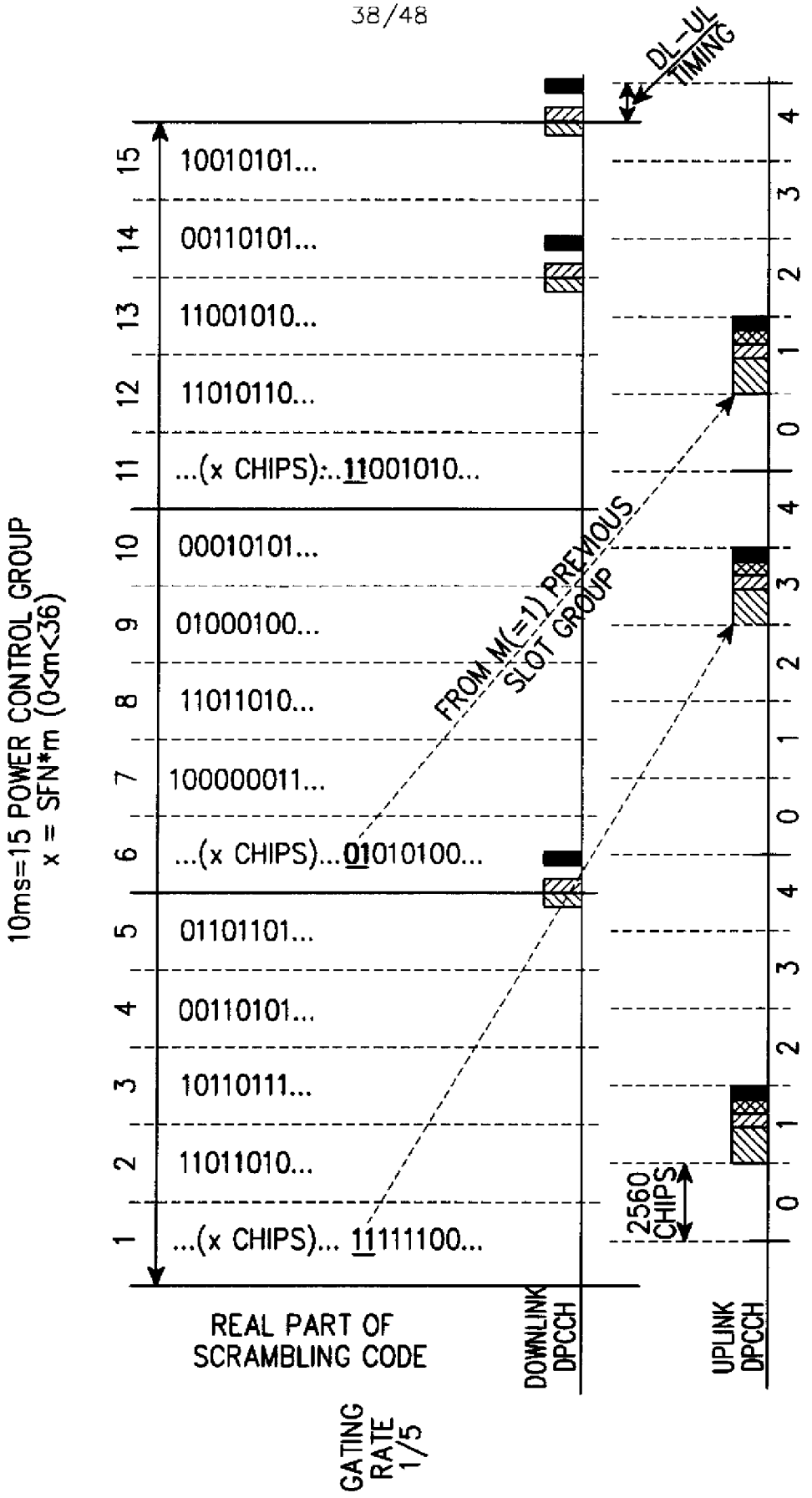

10ms=15 POWER CONTROL GROUP
x = SFN*m (0<m<36)
DL-UL TIMING
15 10010101...
14 00110101...
13 11001010...
12 11010110...
11 ...(x CHIPS):..11001010...
10 00010101...
9 01000100...
8 11011010...
7 100000011...
6 ...(x CHIPS)...01010100...
5 01101101...
4 00110101...
3 10110111...
2 11011010...
1 ...(x CHIPS)... 11111100...
FROM M(=1) PREVIOUS SLOT GROUP
2560 CHIPS
REAL PART OF SCRAMBLING CODE
DOWNLINK DPCCH
UPLINK DPCCH
GATING RATE 1/5

FIG. 14C

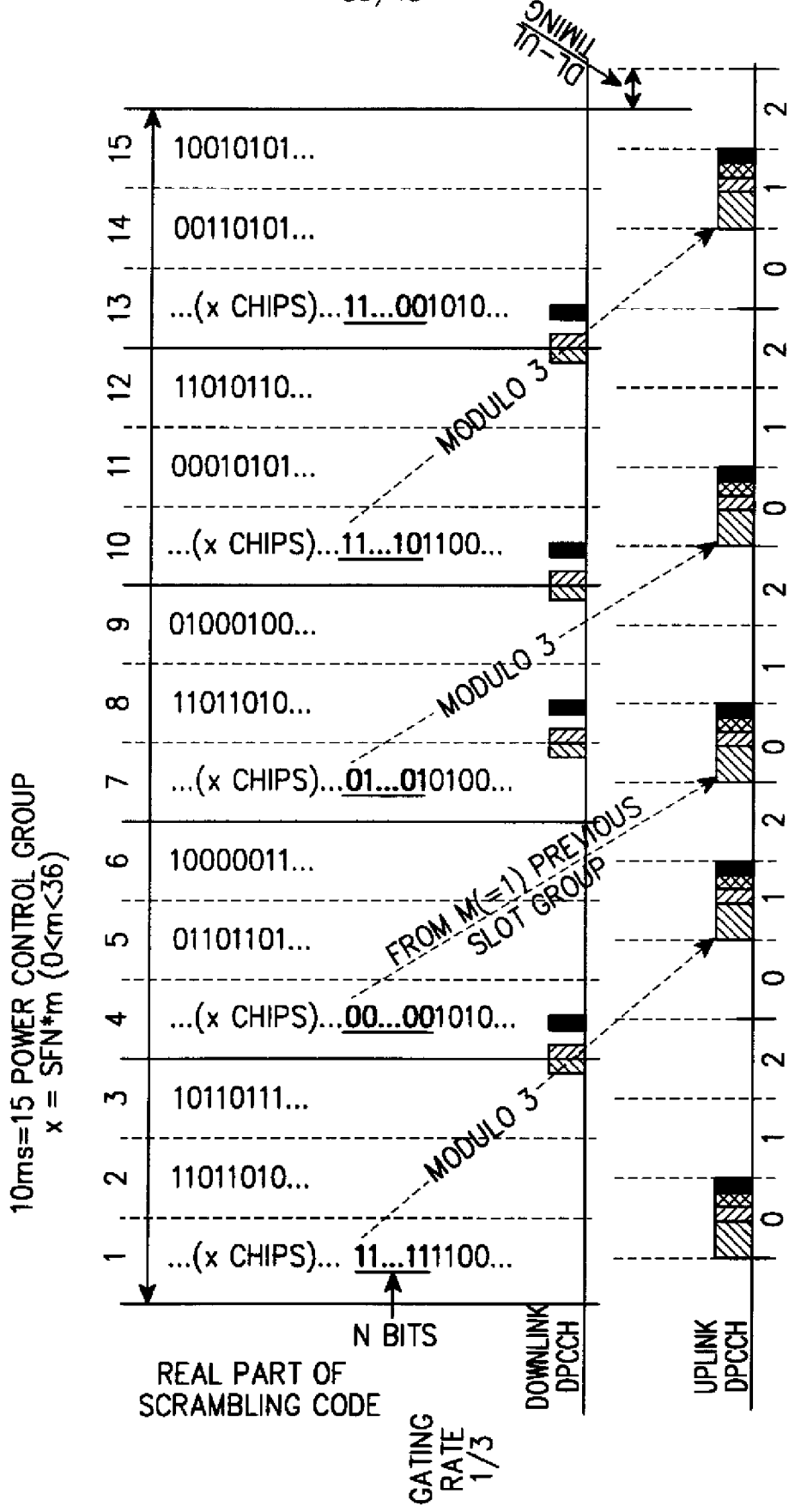

10ms=15 POWER CONTROL GROUP
x = SFN*m (0<m<36)
15 10010101...
14 00110101...
13 ...(x CHIPS)...11...001010...
12 11010110...
11 00010101...
10 ...(x CHIPS)...11...101100...
9 01000100...
8 11011010...
7 ...(x CHIPS)...01...010100...
6 10000011...
5 01101101...
4 ...(x CHIPS)...00...001010...
3 10110111...
2 11011010...
1 ...(x CHIPS)... 11...111100...
MODULO 3
MODULO 3
MODULO 3
FROM M(=1) PREVIOUS SLOT GROUP
N BITS
REAL PART OF SCRAMBLING CODE
GATING RATE 1/3
DOWNLINK DPCCH
UPLINK DPCCH
TIMING UL-DL
2 1 0 2 1 0 2 1 0 2 1 0

FIG. 14D

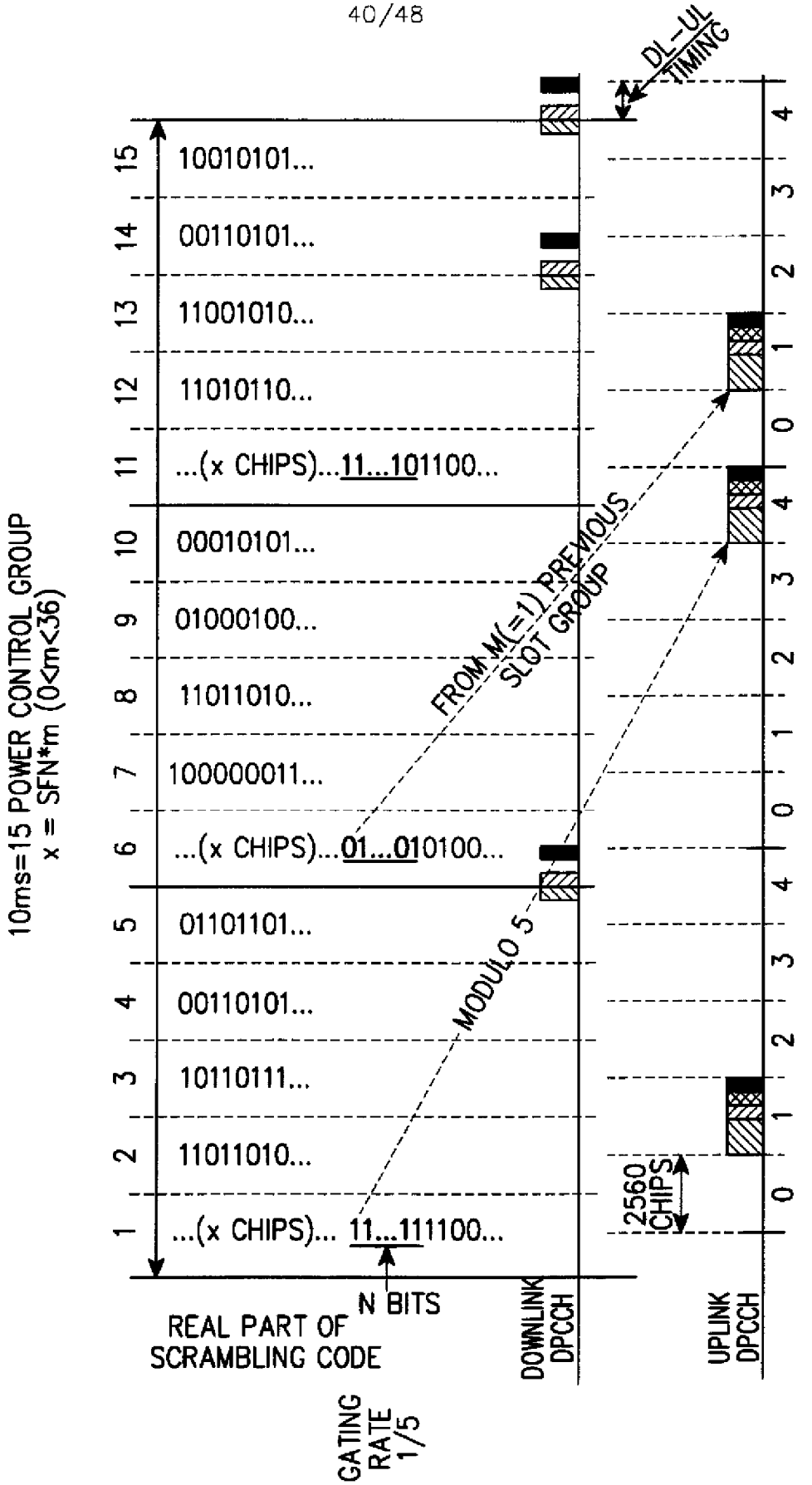

10ms=15 POWER CONTROL GROUP
x = SFN*m (0<m<36)
15 10010101...
14 00110101...
13 11001010...
12 11010110...
11 ...(x CHIPS)...11...101100...
10 00010101...
9 01000100...
8 11011010...
7 100000011...
6 ...(x CHIPS)...01...010100...
5 01101101...
4 00110101...
3 10110111...
2 11011010...
1 ...(x CHIPS)... 11...111100...
N BITS
REAL PART OF SCRAMBLING CODE
GATING RATE 1/5
DOWNLINK DPCCH
UPLINK DPCCH
DL-UL TIMING
FROM M(=1) PREVIOUS SLOT GROUP
MODULO 5
2560 CHIPS
0 1 2 3 4

FIG. 15A

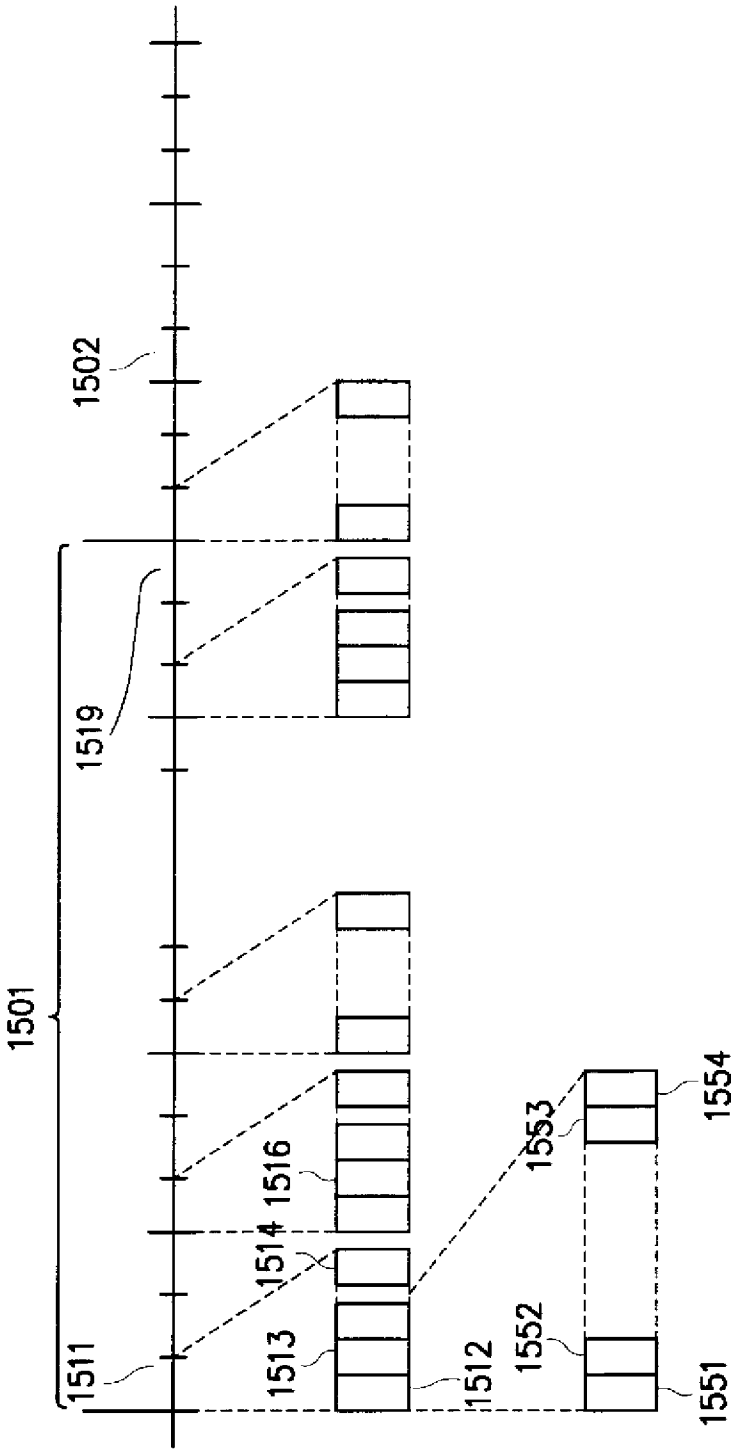


FIG. 15B

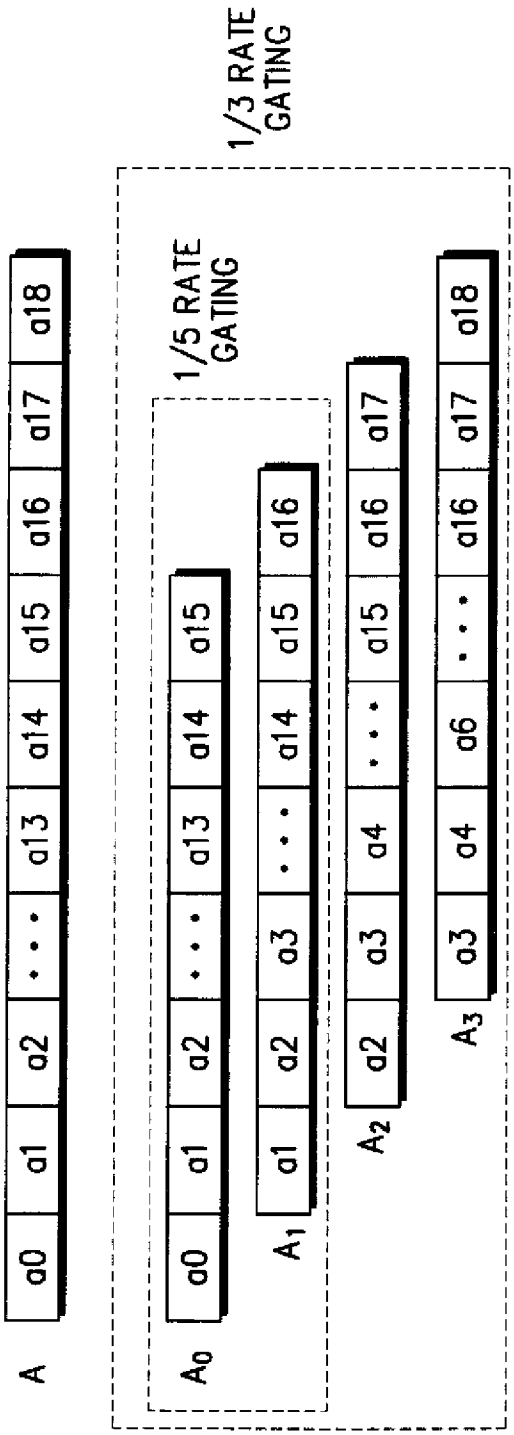

1/3 RATE GATING
1/5 RATE GATING
A
a0 a1 a2 • • • a13 a14 a15 a16 a17 a18
A0
a0 a1 a2 • • • a13 a14 a15
A1
a1 a2 a3 • • • a14 a15 a16
A2
a2 a3 a4 • • • a15 a16 a17
A3
a3 a4 a6 • • • a16 a17 a18

FIG. 15C

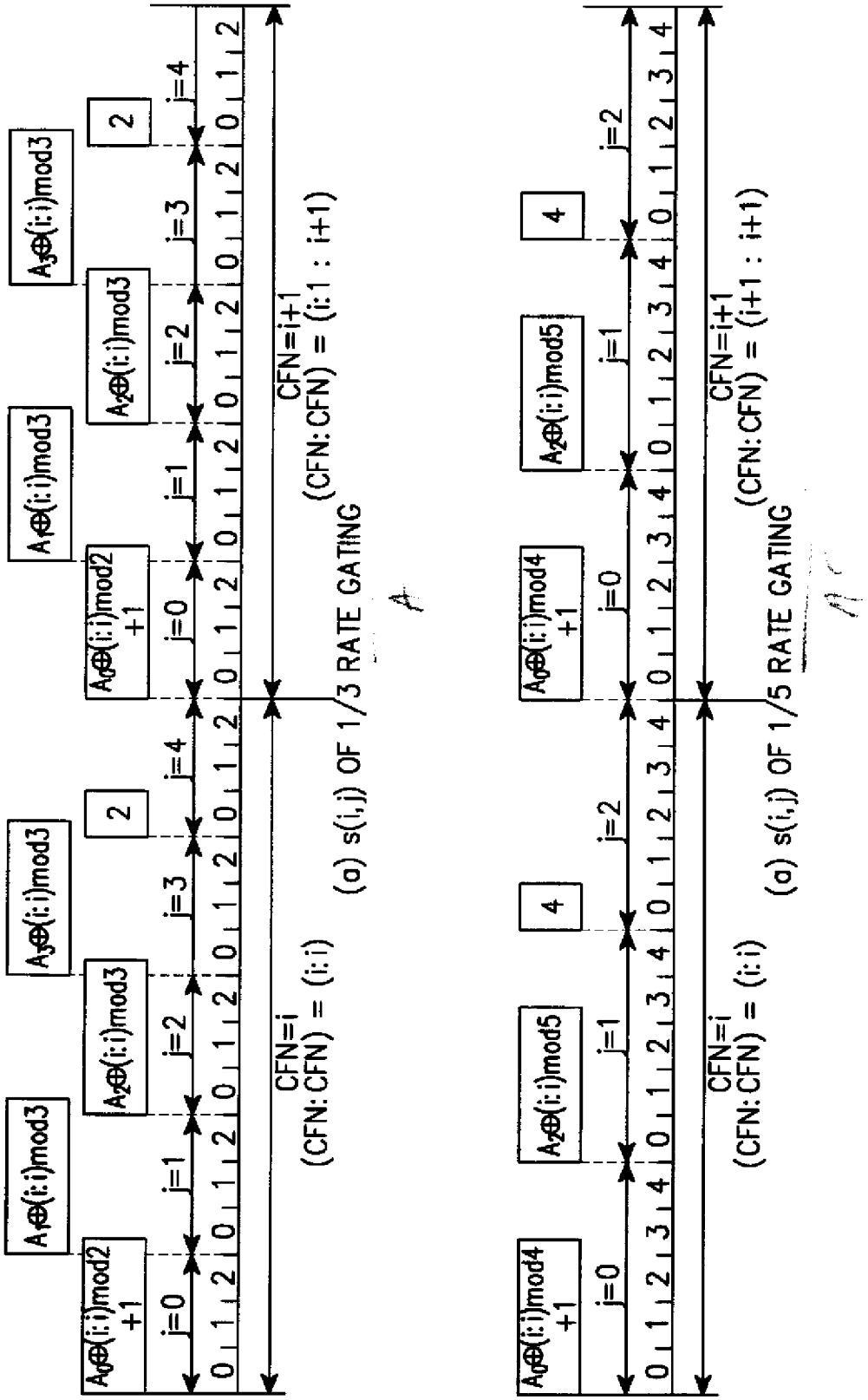

A0⊕(i:i)mod2 +1
A1⊕(i:i)mod3
A2⊕(i:i)mod3
A3⊕(i:i)mod3
2
j=0
j=1
j=2
j=3
j=4
CFN=i
(CFN:CFN) = (i:i)
CFN=i+1
(CFN:CFN) = (i:1 : i+1)
(a) s(i,j) OF 1/3 RATE GATING
A0⊕(i:i)mod4 +1
A2⊕(i:i)mod5
4
CFN=i
(CFN:CFN) = (i:i)
CFN=i+1
(CFN:CFN) = (i+1 : i+1)
(a) s(i,j) OF 1/5 RATE GATING

FIG. 16

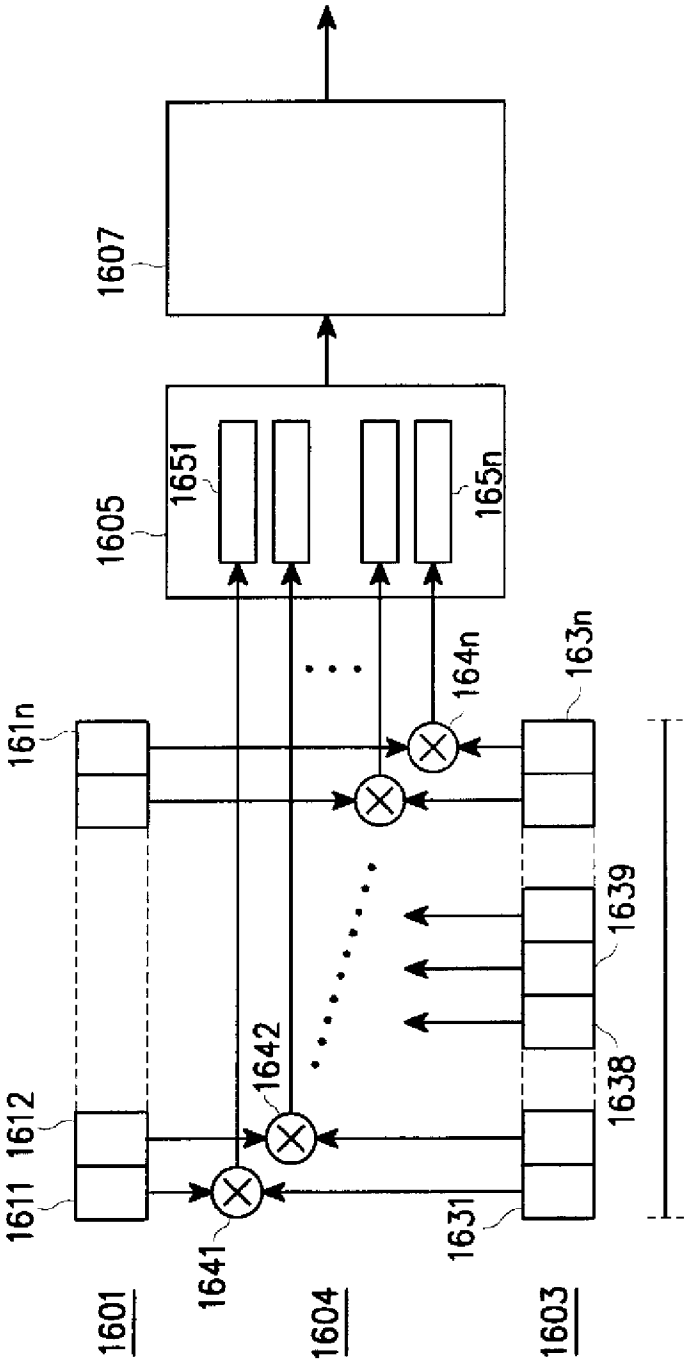

1607
1605
1651
165n
164n
163n
161n
1639
1642
1638
1612
1611
1641
1631
1601
1604
1603

FIG. 17A

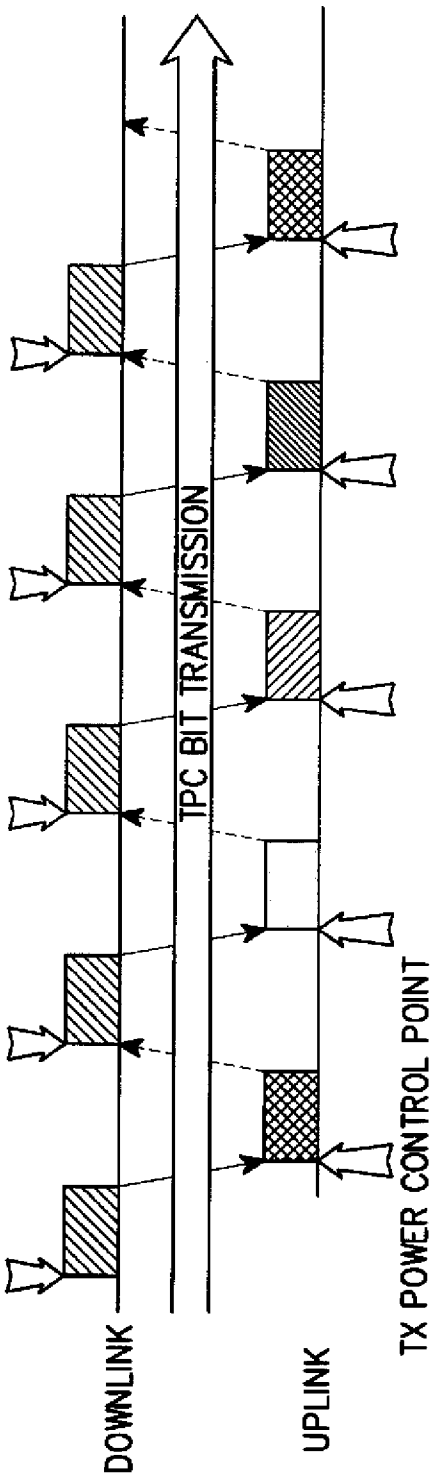

TPC BIT TRANSMISSION
DOWNLINK
UPLINK
TX POWER CONTROL POINT

FIG. 17B

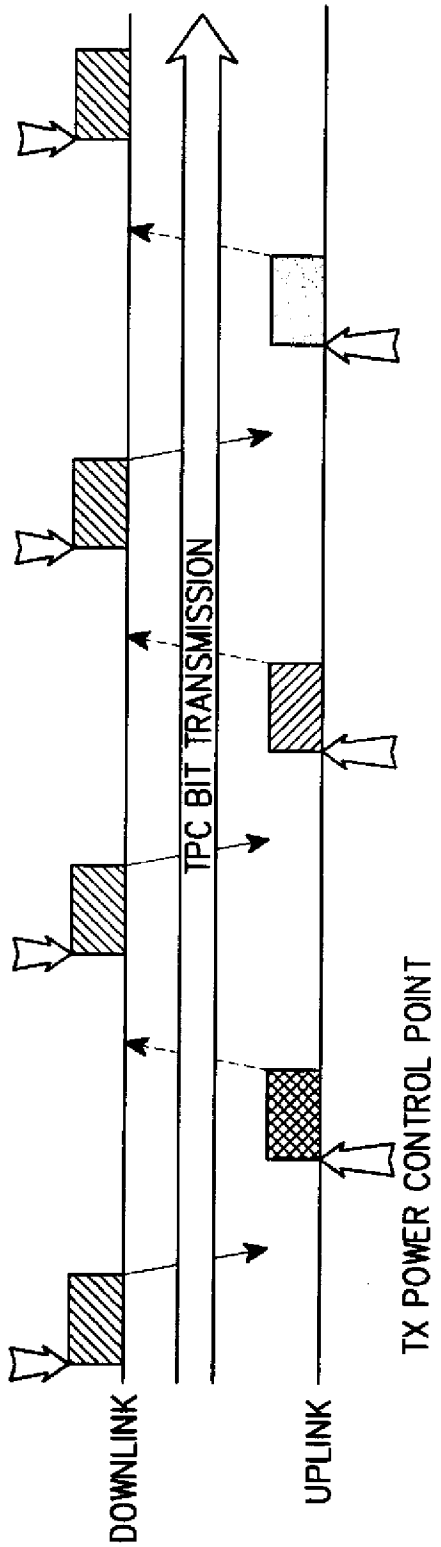

TPC BIT TRANSMISSION
DOWNLINK
UPLINK
TX POWER CONTROL POINT

FIG. 18A

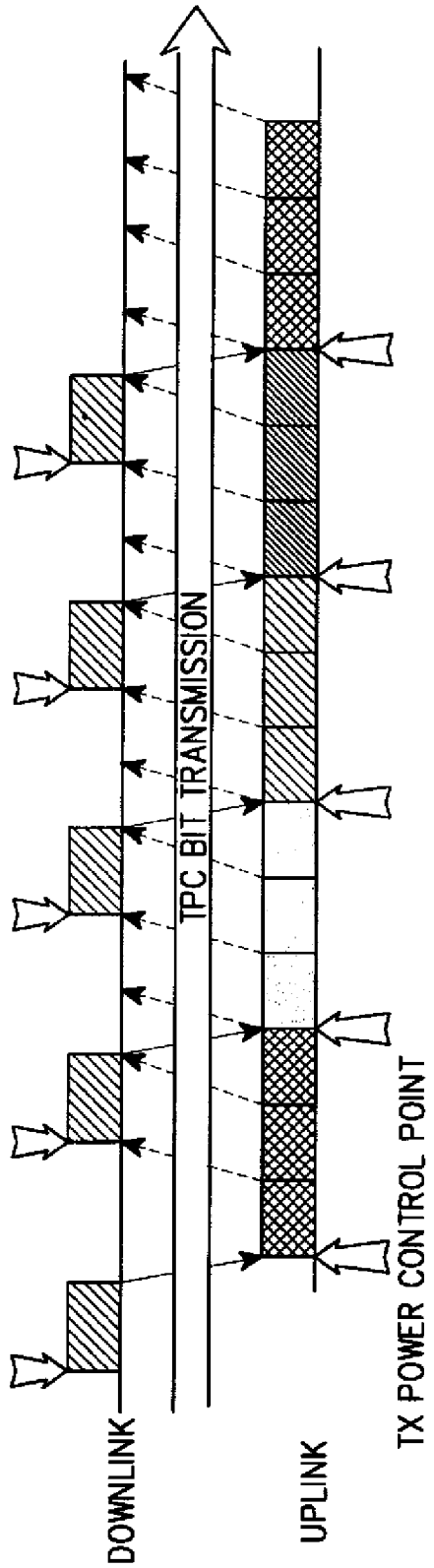
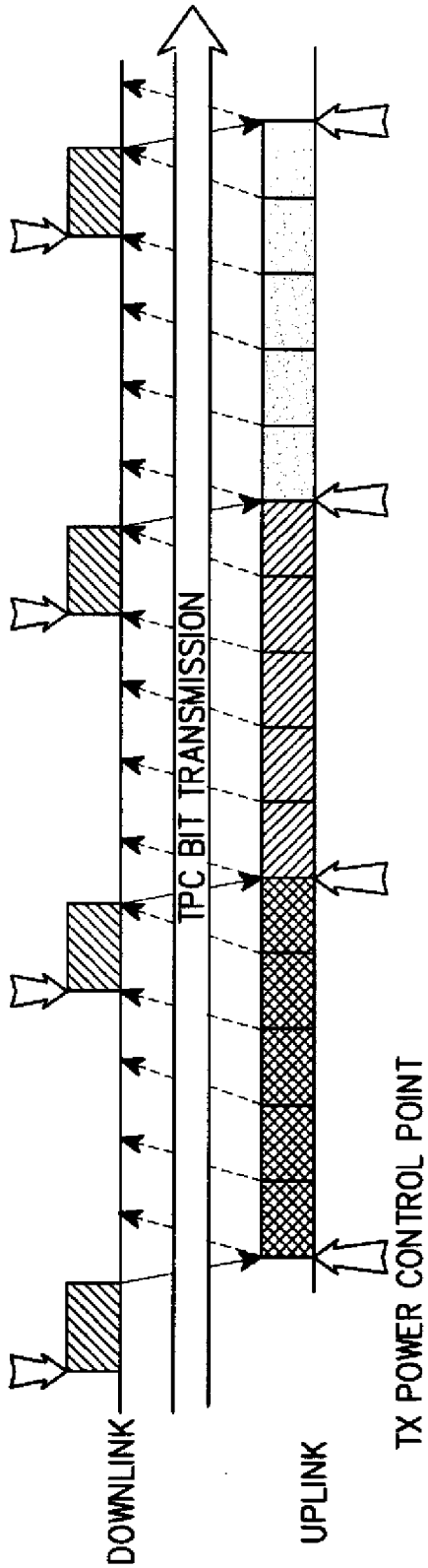

TPC BIT TRANSMISSION
DOWNLINK
UPLINK
TX POWER CONTROL POINT

FIG. 18B


TPC BIT TRANSMISSION
DOWNLINK
UPLINK
TX POWER CONTROL POINT

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR00/01100

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H04J 13/00, H04B 1/69

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimun documentation searched (classification system followed by classification symbols)

KE, JP, US, EP classes as above

Documentation searched other than minimun documentation to the extent that such documents are included in the fileds searched

Korean Patents and applications for inventions since 1975
Korean Utility models and applications for Utility models since 1975

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search trerms used)

NPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KE 10-89-0001308(General Electric company) 20 MAR. 1989 abstract, claims 1 ~ 12,fig 10, 11	1, 2, 13, 15, 19, 21,27
A	US 4,787,095(Advanced Micro Devices) abstract	1-5, 13,19,21,27-31

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 JANUARY 2001 (19.01.2001)	19 JANUARY 2001 (19.01.2001)

Name and mailing address of the ISA/KR	Authorized officer
Korean Industrial Property Office Government Complex-Taejon, Dunsan-dong, So-ku, Taejon Metropolitan City 302-701, Republic of Korea	JEONG, Yong Joo
Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-5674

Form PCT/ISA/210 (second sheet) (July 1998)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 October 2002 (17.10.2002)

PCT

(10) International Publication Number
WO 02/082689 A2

(51) International Patent Classification[7]: H04B 7/06, 7/08

(21) International Application Number: PCT/US02/10599

(22) International Filing Date: 5 April 2002 (05.04.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/281,985 7 April 2001 (07.04.2001) US
10/113,699 1 April 2002 (01.04.2002) US

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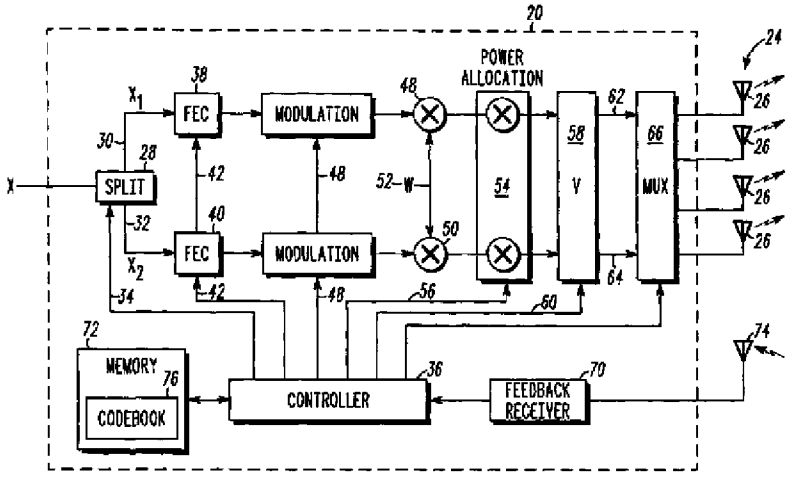
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
without international search report and to be republished upon receipt of that report

[Continued on next page]

(54) Title: METHOD AND SYSTEM IN A TRANSCEIVER FOR CONTROLLING A MULTIPLE-INPUT, MULTIPLE-OUTPUT COMMUNICATIONS CHANNEL



(57) Abstract: The present invention makes it possible to increase a data rate between a transmitter and receiver using a multiple-input, multiple-output radio frequency channel. A multiple-stream, multiple-antenna receiver measures a composite channel between a multiple-antenna transmitter and a multiple-antenna receiver to produce a composite channel measurement. The receiver selects a plurality of antenna array weight sets for use in the multiple-antenna transmitter in response to the composite channel measurement, where each antenna array weight set is associated with one of multiple data streams. Information describing the plurality of antenna array weight sets for use in the multiple-antenna transmitter are then transmitted.

WO 02/082689 A2

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

METHOD AND SYSTEM IN A TRANSCEIVER FOR CONTROLLING A MULTIPLE-INPUT, MULTIPLE-OUTPUT COMMUNICATIONS CHANNEL

Field of the Invention

The present invention is related in general to communication systems, and more particularly to a method and system for controlling the transmitting and receiving of multiple data streams in a multiple-input, multiple-output communications channel.

Background of the Invention

Communication system designers are always looking for ways to increase the capacity of a communications channel between a transmitter and receiver. A communications channel may be defined as a system that transmits a sequence of symbols from one point to another. For example, a cellular communications system includes a channel for wirelessly transmitting a sequence of symbols that represent voice or data, back and forth between the telephone system and subscriber unit. An increase in the capacity of this channel means an increase in the rate of transmitting symbols. And when more symbols are transmitted in the same amount of time, voice can sound better, and it may take less time to transfer data files.

To increase the capacity of a wireless communications channel, antenna arrays have been used at the transmitter to better focus the transmitted energy at the receiver. An antenna array is a group of

spaced apart antennas that each transmit an antenna signal that has a specific gain and phase relationship with the other antenna signals. When the antennas work together transmitting the antenna signals, they produce an antenna pattern that is more focused on the receiver than a pattern produced by a single antenna. Note that the process of changing the gain and phase of a signal to produce antenna signals may be referred to as "weighting" the signal using a set of "antenna array weights."

Because antenna arrays may similarly be used at a receiver to improve signal quality, use of antenna arrays at both the transmitter and receiver has also been proposed to increase channel capacity. When multiple antennas are used at the transmitter and receiver, the wireless channel between them may be referred to as a multiple-input, multiple-output (MIMO) channel.

Fig. 1 shows a high-level schematic diagram of a communications channel, wherein a portion of the communications channel is wireless. As shown, x represents user data that will be wirelessly transmitted to the receiver. At the receiver, x is represented as an estimate of the data, $\hat{x}$. User data x may be split to produce a vector that represents multiple data streams, x_1, x_2, ...

User data x is processed by matrix **V** to produce adaptive array antenna signals z. Each column of matrix **V** is a vector containing an antenna array weight set used to transmit one of the data streams x_i. Signals z are transmitted from antenna elements of the antenna array, through the air, and received at the receiver antenna array as received antenna signals r. The air interface between antenna signals z and received antenna signals r includes matrix H, which describes the effects of the air interface on signals z. The air interface is also described by the addition of noise n to signals z.

Received antenna signals r are processed in the receiver by matrix U' to produce the estimate of data, $\hat{\mathbf{x}}$.

With reference now to **Fig. 2**, there is depicted a two-input, two-output MIMO antenna array system. This MIMO system may be used to simultaneously transmit two different data streams, x_1 and x_2, to a single subscriber unit through a "composite channel" **H**, defined by the matrix

$$\mathbf{H} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix}$$

where h_{ij} , $i = 1,2$, $j = 1,2$ are complex channel values. Note that the term "composite channel" as used herein refers to a complete measurement or description of a channel, wherein the effects of all combinations of transmit antennas and receive antennas are considered. The composite channel may be thought of as the aggregation of all channels between pairs of single antennas, defined by all pair-wise combinations of transmit and receive antennas.

When a flat Rayleigh fading channel is assumed, h_{ij} are complex-valued Gaussian numbers with unity average power, $E\left[h_{ij}h_{ij}^*\right] = 1$. The received (baseband) vector **r** (see **FIG. 1**) can be written as follows

$$\mathbf{r} = \mathbf{H}\mathbf{x} + \mathbf{n}$$

where $\mathbf{x} = \begin{bmatrix} x_1 & x_2 \end{bmatrix}^T$ is the vector of transmitted data streams, and **n** is a vector of noise samples, with additive white Gaussian noise with variance σ_n^2.

Note that in a noise free channel, both streams can be recovered perfectly if channel matrix **H** is full rank. That is, two equations and two unknowns can be solved to recover the unknowns $\mathbf{x} = [x_1 \quad x_2]^T$. When $\mathbf{x} = \mathbf{H}^{-1}\mathbf{r}$, both data streams can be recovered and link, or channel, capacity can be doubled. For example, a linear architecture may use zero forcing receivers to multiply the received vector **r**, with $\mathbf{H}^{-1}$. This works well with a high signal-to-noise ratio (SNR), but with a low SNR it boosts noise, which is not desirable.

In another linear receiver architecture, a Minimum Mean Square Error (MMSE) receiver may be used to minimize the average difference between detected data streams and the received signal.

While linear and non-linear receiver architectures can both be implemented to detect the multiple streams in noisy channels, in practical applications, noise in the channel will often require the use of non-linear receivers, which are more complicated and expensive to build. Examples of non-linear receivers with improved performance are Serial-Interference-Cancellation (SIC) receivers and a Maximum Likelihood (ML) receivers. Because of their complexity and cost, non-linear receivers should be avoided if possible.

Theoretical MIMO Capacity:

The capacity of a MIMO system may be shown with the following analysis. Suppose the Singular Value Decomposition (SVD) of the channel matrix **H** is given by

$$\mathbf{H} = \mathbf{USV}' \qquad (1)$$

where **S** is a diagonal matrix composed of the singular values (i.e., the square-roots of eigenvalues of $\mathbf{H}'\mathbf{H}$ or $\mathbf{HH}'$), **U** is an orthogonal matrix

with column vectors equal to the eigenvectors of $\mathbf{HH}'$, $\mathbf{V}$ is an orthogonal matrix with columns equal to the eigenvectors of $\mathbf{H}'\mathbf{H}$, and the "$'$" operator is the complex conjugate transpose operation. As an example, consider the following composite channel matrix

$$\mathbf{H} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \tag{1.1}$$

The SVD of this composite channel is

$$\mathbf{H} = \mathbf{USV}' = \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} \\ 1/\sqrt{2} & -1/\sqrt{2} \end{bmatrix} \begin{bmatrix} \sqrt{2} & 0 \\ 0 & \sqrt{2} \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{1.2}$$

Referring to **Fig. 1**, the transmit vector is

$$\mathbf{z} = \mathbf{Vx} \tag{2}$$

Thus, the received vector is

$$\mathbf{r} = \mathbf{Hz} + \mathbf{n} \tag{3}$$

Replacing $\mathbf{H}$ and $\mathbf{z}$ with (1) and (2), we get

$$\mathbf{r} = \mathbf{USV}'\mathbf{Vx} + \mathbf{n} = \mathbf{USx} + \mathbf{n} \tag{4}$$

where, since $\mathbf{V}$ is an orthonormal matrix, $\mathbf{V}'\mathbf{V}$ is replaced with identity. Next, the received vector is pre-multiplied with $\mathbf{U}'$:

$$\begin{aligned} \hat{\mathbf{x}} &= \mathbf{U}'\mathbf{USx} + \mathbf{U}'\mathbf{n} \\ &= \mathbf{Sx} + \mathbf{e} \end{aligned} \tag{5}$$

Again, since $\mathbf{U}$ is an orthonormal matrix, $\mathbf{U}'\mathbf{U}$ is replaced with identity. Note that the new noise vector, $\mathbf{e}$, has the same covariance

matrix as **n**, because pre-multiplication with an orthonormal matrix does not alter the noise covariance.

If equation (5) is rewritten for the case of 2 transmit antennas, and 2 receive antennas it becomes:

$$\begin{bmatrix}\hat{\mathbf{x}}_1\\ \hat{\mathbf{x}}_2\end{bmatrix}=\begin{bmatrix}\sqrt{\lambda_1} & 0\\ 0 & \sqrt{\lambda_2}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\begin{bmatrix}e_1\\ e_2\end{bmatrix}=\begin{bmatrix}\sqrt{\lambda_1}x_1+e_1\\ \sqrt{\lambda_2}x_2+e_2\end{bmatrix} \quad (6)$$

where λ_i are the channel matrix eigenvalues.

The error free channel capacity based on the Shannon bound is well known, and is given by

$$C_1=\log_2(1+\rho) \quad \text{bits/symbol} \quad (7)$$

where ρ is the channel SNR. From (5) and (6), note that the MIMO channel capacity based on the Shannon bound is the sum of the capacities per data stream:

$$C_{\text{MIMO}}=\sum_{i=1}^{M}C_i=\sum_{i=1}^{M}\log_2\left(1+\frac{\rho}{M}\lambda_i\right) \quad \text{bits/symbol} \quad (8)$$

where M is the minimum number of antennas at either the transmitter or the receiver. For the 2 transmit antenna, 2 receive antenna example, M=2. It is important to note that in (8), the total transmit power has been normalized such that it remains the same for any number of transmit antennas. The ratio ρ/M ensures equal power transmitted on all antennas, and it maintains the same total power for all values of M.

In general, equal power transmission of (8) is sub-optimal. The total capacity, which is the sum of each data stream capacity, $C_{MIMO} = \sum_i C_i$, can be maximized by increasing the power to the high SNR streams, and reducing the power to the low SNR streams, such that the total transmit power remains the same. This procedure is typically referred to as "waterfilling."

By including waterfilling weights for optimum power allocation per data stream, (8) becomes:

$$C_{MIMO} = \sum_{i=1}^{M} \log_2\left(1 + \frac{\rho}{M}\lambda_i w_i\right) \quad \text{bits/symbol} \qquad (9)$$

where waterfilling weights are computed from

$$\sum_i w_i = \sum_i \max\left[0, \left(K - \frac{\sigma_n^2}{\lambda_i}\right)\right] = 1,$$

which is the waterfilling criterion, which is discussed by R.G. Gallager in *Information Theory and Reliable Communication,* New York: John Wiley & Sons, 1968. Here, K is a constant determined by iterations, and w_i are set accordingly.

Because transmitters in prior art systems lack data regarding the conditions of the composite channel, the performance of these systems cannot approach the Shannon bound for the MIMO channel. Furthermore, the amount of data needed to describe a composite MIMO channel is large, which would consume a large percentage of channel capacity when communicated to the transmitter.

Thus, it should be apparent that a need exists for an improved method and system for using feedback to efficiently control data

transmission and reception in a multiple-input, multiple-output radio frequency channel.

Brief Description of the Drawings

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, further objects, and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a high-level schematic diagram of a communications channel, wherein a portion of the communications channel is wireless;

FIG. 2 is a high-level block diagram of a two-input, two-output MIMO channel;

FIG. 3 is a block diagram of a multiple-stream, multiple-antenna transmitter that may be used to implement the method and system of the present invention;

FIG. 4 is a more detailed block diagram of antenna array signal processor;

FIG. 5 depicts a receiver for use in a multiple-stream, multiple-antenna transceiver system in accordance with the method and system of the present invention;

FIG. 6 is a high-level logic flowchart that illustrates a feedback method in a multiple-stream, multiple-antenna receiver in accordance with the method and system of the present invention;

FIG. 7 is a high-level logic flow chart that illustrates a feedback method in a multiple-stream, multiple-antenna transmitter in accordance with the method and system of the present invention;

FIG. 8 is a more detailed logical flow chart that illustrates the process for estimating a composite channel and selecting array weight sets in accordance with the method and system of the present invention;

FIG. 9 shows simulation results comparing quantized MIMO feedback with un-quantized, ideal MIMO feedback, in accordance with the method and system of the present invention; and

FIG. 10 shows simulation results for a MIMO transceiver system in accordance with the method and system of the present invention.

Detailed Description of the Invention

With reference now to **FIG. 3**, there is depicted a multiple-stream, multiple-antenna transmitter that may be used to implement the method and system of the present invention. As illustrated, transmitter **20** receives user data **22** and transmits user data **22** using antenna array **24**, which comprises antenna elements **26**.

User data **22** enters data splitter **28**, which separates the user data stream into a plurality of data streams, such as data stream **30** and data stream **32**. While two data streams are shown in **FIG. 3**, data splitter **28** may produce any number of data streams. Data splitter **28** splits data in proportion to control signal **34**, which is produced by controller **36**. For example, control signal **34** may specify a ratio of 2-to-1, wherein two bits are sent to data stream **30** and one bit is sent to data stream **32**. This splitting ratio may specify an equal number of bits on both streams, or all data bits are sent to one stream.

Data streams **30** and **32** output by data splitter **28** are input into error correction encoders **38** and **40**. These error correction encoders may be implemented with a convolutional encoder, a turbo encoder, a block encoder, or the like. The type of encoding, and the rate of encoding is controlled by control signal **42**, which is output by controller **36**. Note that control signal **42** may set error correction encoders **38** and **40** to the same error encoding schemes, or different encoding schemes.

Outputs of error correction encoders **38** and **40** are coupled to inputs of modulators **44** and **46**. Modulators **44** and **46** may be implemented with linear or non-linear modulation schemes, including

all varieties of modulators that modulate amplitude and phase, and combinations of amplitude and phase. Examples of modulators that may be used include Binary Phase Shift Keying modulators (BPSK), Quadrature Phase Shift Keying modulators (QPSK), M-ary phase shift keying modulators, M-ary quadrature amplitude modulators (MQAM), and the like.

Control signal **48** selects the type of modulation used in modulators **44** and **46**. Control signal **48** is produced by controller **36**. According to the present invention, the modulation schemes in the data streams may be the same, or different.

The output of modulators **44** and **46** are coupled to inputs of spreaders **48** and **50**, respectively. Spreaders **48** and **50** spread the signal using spreading code **52**, wherein the spreading code is assigned to user data **22**.

Outputs of spreaders **48** and **50** are coupled to inputs of power allocator **54**. Power allocator **54** sets a power ratio between data streams **30** and **32** in response to control signal **56** from controller **36**. Power allocator **54** may allocate all power to one data stream, equal powers on data streams, or other ratios of unequal power allocations.. Power allocator **54** does not allocate power to data streams **30** and **32** relative to data streams belonging to other user data not shown in **FIG. 3**. This means that power allocator **54** does not allocate an absolute level of power to a user. The absolute power allocated to each data stream, and each user, is determined by available power in power amplifiers and other control functions not shown in **FIG. 3**.

Outputs of power allocator **54** are coupled to inputs of antenna array signal processor **58**, which further processes the data streams

by applying antenna array weight sets to each data stream. These antenna array weight sets come from controller **36** via control signal **60**. By applying the antenna array weight sets to data streams **30** and **32**, antenna array signal processor enables the transmission of each data stream with a different antenna array pattern.

The outputs of antenna array signal processor **58** include weighted components of the input data streams. For example, output **62** may include a phase-and-gain weighted portion of data stream **30** added together with a phase-and-gain weighted portion of data stream **32**. The number of weighted outputs from antenna array signal processor **58** may be equal to or greater than the number of data streams. While the number of outputs of antenna array signal processor **58** may be greater than the number of data streams input, the number of data streams transmitted remains the same.

With reference now to **FIG. 4**, there is depicted a high-level block diagram of antenna array signal processor **58**. As shown, data streams **30** and **32** enter antenna array signal processor **58**, wherein a copy of each data stream is sent to a gain multiplier corresponding to an antenna element that will be used in an antenna array. In the example shown in **FIG. 4**, two antennas will be used in the antenna array, therefore copies of each data stream are sent to two gain multipliers **80**.

Following each gain multiplier **80** is a phase shifter **82**, which rotates the phase of the signal according to a control signal input. Outputs of phase shifters **82** are coupled to summers **84**, which add the weighted data streams to produce output signals **62** and **64**.

Control signal **60** (see **FIG. 3**) includes a plurality of antenna array weight sets, wherein one antenna array weight set is associated

with each data stream. For example, control signal **60** includes weight set signals **86** and **88**. Weight set signal **86** includes gain and phase weights (i.e., complex weights) for each gain multiplier **80** and phase shifter **82** associated with data stream **30**. Thus, the outputs of phase shifters **82** associated with data stream **30** produce antenna signals that provide a selected antenna pattern for data stream **30**. Similarly, weight set signal **88** includes phase and gain weights for each gain multiplier **80** and phase shifter **82** associated with data stream **32**. In the outputs of phase shifters **82** associated with data stream **32** produce antenna signals for driving an antenna array with a selected pattern for data stream **32**.

In order to produce desired antenna patterns for each data stream, gain multipliers **80** associated with a data stream may have different gain values and phase shifters **82** associated with a data stream may have different phase shift values, whereby producing antenna signals that work together to form a particular transmission pattern.

In some embodiments of transmitter **20**, output signals **62** and **64** may be up-converted, amplified, and coupled to two antenna elements **26**. However, in the embodiment shown in **FIG. 3**, multiplexer **66** is used to couple output signals **62** and **64** to selected antenna elements **26** in response to control signal **68** from controller **36**. This means that control signal **62** may be coupled to any one of antenna elements **26** in antenna array **24**, while output signal **64** is coupled to one of the remaining antenna elements **26**.

Controller **36** outputs control signals **34**, **42**, **48**, **56**, **60**, and **68** based upon information received from feedback receiver **70**, and data stored in memory **72**. Feedback receiver **70** is shown coupled to antenna **74** for receiving feedback data from a remote receiver, such

as the receiver shown in **FIG. 5**. While antenna **74** is shown separate from antenna array **24**, one of the antenna elements **26** of array **24** may be used to receive the feedback data.

Feedback data from feedback receiver **70** may include a codebook index, which may be used by controller **36** to lookup transmission parameters in codebook **76** within memory **72**.

Controller **36** may also be used to calculate, or derive, additional control signals or transmission parameters based upon feedback data. Therefore, it should be understood that feedback data may include measurements upon which calculations may be based, or data that indicates parameters to be used in transmitter **20**.

With reference now to **FIG. 5**, there is depicted a receiver for use in a multiple-stream, multiple-antenna transceiver system in accordance with the method and system of the present invention. As shown, receiver **98** includes antenna array **100** having elements **102** that receive radio frequency signals **104** and **106**. Received RF signals **104** and **106** are most likely different signals because antenna elements **102** are spaced apart, and propagation paths taken by received RF signals **104** and **106** from antenna elements **26** of transmitter **20** are most likely different in a multi-path fading environment.

In the multiple-stream, multiple-antenna transceiver system that is made up of transmitter **20** and receiver **98**, multiple data streams are transmitted to increase the data throughput between transmitter **20** and receiver **98**. Transmitter **20** is able to simultaneously transmit multiple data streams, and receiver **98** is able to keep the multiple streams separate by exploiting the differences in the channel characteristics between the multiple

antennas at transmitter **20** and receiver **98**. Thus, user data **22** in transmitter **20** is received by receiver **98** and output as estimated user data **108**.

Received RF signals **104** and **106** are input into radio frequency receiver front end **110**, wherein the radio frequency signals are down converted and digitized. The output of radio frequency receiver front end **110** is a stream of complex baseband digital samples that represent received RF signals **104** and **106**.

The outputs of radio frequency receiver front end **110** are input into receiver signal processor **112**, which has the function of separating data streams **30** and **32** (See **FIG. 3**) in receiver **98**. In one embodiment of the present invention, receiver signal processor **112** may be implemented by multiplying the input signals by the complex conjugate transpose of the **U** matrix, which is the left singular vectors of the singular value decomposition of the composite channel matrix **H**. Receiver signal processor **112** is controlled by control signal **115** from controller **113**.

The data streams output by receiver signal processor **112** are input to despreaders **114** and **116**, which despread the signals using spreading code **52**, which is the same spreading code used in the transmitter. The outputs of despreader **114** and **116** are coupled, respectively, to the inputs of demodulator and decoders **118** and **120**. Each demodulator and decoder **118** and **120** demodulates the signal and decodes the signal using demodulation and error correction decoding techniques that compliment those selected for each data stream in the transmitter. Thus, the type of demodulator and decoder functions used depends upon what was used in transmitter **20**, as indicated by control signal **122** from controller **113**. Demodulators

and decoders **118** and **120** may be the same function, or may be different functions.

The outputs from demodulator and decoder **118** and **120** are input into combiner **124**, which combines the multiple streams received back into a single stream for output as estimated user data **108**. Combiner **124** operates under the control of controller **113**, as directed by control signal **126**. Because the received data streams may have different data rates, and because one data stream may have a data rate equal to zero, combiner **124** must reconstruct the user data in accordance with the way data was originally split by data splitter **28** in transmitter **20** in **FIG. 3**.

In order to control the transmission of multiple data streams via multiple antennas at the transmitter, receiver **98** must measure the composite channel and send feedback data to the transmitter. As shown, outputs of radio frequency front end **110** are also coupled to composite channel estimator **128**, which uses pilot signals transmitted from each antenna element **26** in transmitter **20** to measure the composite channel between the multiple input antennas and multiple output antennas. The function of composite channel estimator **128**, and many of the other functional blocks in the data feedback portion of receiver **98**, are described in more completely in reference to **FIG. 8**, below.

The output of composite channel estimator **128**, which is represented by the **H** matrix, is input into **V** matrix computer and selector **130**. The "computing function" of block **130** computes **V**, which is a matrix describing desired antenna array weight sets to be used for each data stream in transmitter **20**. The desired antenna array weight sets are computed based upon the composite channel measurement.

The "selector function" of block **130** is a quantizing function that selects antenna array weight sets that most closely match the desire antenna array weight sets. By performing quantization, the amount of feedback data required to instruct transmitter **20** how to transmit over the MIMO channel may be reduced.

The selected antenna array weight sets output by computer and selector **130** are input into SNR computer and power allocator **132**, wherein a signal to noise ratio is computed for each data stream hypothetically transmitted using the selected antenna array weight sets. Based upon the SNR computations, the power allocation function of block **132** allocates power to each data stream, wherein the power is allocated to maximize the data throughput based upon a waterfilling algorithm. Once power has been allocated to each data stream, final SNR calculations may be performed using the selected power allocation.

Modulator and coder **134** receives information from SNR computer and power allocator **132** that it uses to select an encoding scheme and a modulation scheme to be used in transmitter **20**. Generally, higher order modulators are selected for data streams having high signal-to-noise ratios.

Feedback transmitter **136** receives information from the **V** matrix computer and selector **130**, SNR computer and power allocator **132**, and modulator and coder selector **134**. This data represents calculations and selections made in receiver **98** that will be used to control the transmission modes of transmitter **20**. In a preferred embodiment, feedback transmitter **136** analyzes the data and selects a codebook value associated transmitter parameters that most closely match the transmitter parameters represented by the input data. Therefore, feedback transmitter **136** may include codebook **138** for

producing a codebook value that is transmitted to transmitter **20** via antenna **140**. Although antenna **140** is shown separate from receive antenna array **100**, antenna **140** may be one of the antenna elements **102** in receive antenna array **100**. Data transmitted by feedback transmitter **136** is received in transmitter **20** by feedback receiver **70**.

With reference now to **FIG. 6**, there is depicted a high-level logic flowchart that illustrates a feedback method in a multiple-stream, multiple-antenna receiver in accordance with the method and system of the present invention. As illustrated, the process begins at block **300**, and thereafter passes to block **302** wherein the composite channel between the multiple-antenna transmitter and the multiple-antenna receiver is measured. This measurement results in the formation of the **H** matrix that is made up of complex channel values, representing gains and phases, as discussed above in reference to **FIG. 2**. The composite channel measurement is made by analyzing received antenna signals **r** (See **FIG. 1**) that include received pilot signals transmitted by each antenna at the transmitter.

Next, the process selects an antenna array weight set associated with each data stream in response to the composite channel measurement, as depicted at block **304**. Note that each simultaneously transmitted data stream has an associated set of weights that are used for each array antenna at the transmitter. Each antenna array weight set is used to produce an antenna pattern for the associated data stream.

In a preferred embodiment, selected antenna array weight sets are determined by calculating the right singular vectors of the SVD of composite channel matrix **H**. This process is more completely described with reference to **FIG. 8**. To reduce the amount of data needed to represent the antenna array weight sets, the desired weight

sets are compared to weight sets in a codebook, and one or more codebook weight sets having the closest distance are selected. The codebook indicator may represent a single antenna array weight set, or a combination of antenna array weight sets.

Note that if predefined combinations of antenna array weight sets are used, a first amount of information may be transmitted to describe a first antenna array weight set, and a second amount of information may be transmitted to describe a second antenna array weight set, wherein the second amount of information may be less than the first amount of information. Similarly, if a second antenna array weight set is restricted, or constrained, to a have a predefined relationship to a first antenna array weight set, the amount of information needed to describe the second set is less than that needed to describe the first.

Once selected, the antenna array weight sets are transmitted to the transmitter, and the transmitter uses the weights to produce selected antenna patterns for each data stream, as illustrated at block **306**. Because of the volume of data that may be needed to represent a complex weight for each antenna, for each data stream, it may be advantageous to use techniques that reduce the number of data bits transmitted from the receiver to the transmitter. As mentioned above, a codebook may be used to store several predefined antenna array weight sets. The number of antenna array weight sets available will determine the resolution of the quantizing process that takes an ideal set of weight sets and maps it to one of the available antenna array weight sets. Note that quantizing errors may become excessive if the number of available antenna array weight sets is too small.

As mentioned above, another way to reduce the amount of feedback data is to constrain the transmitter to transmitting antenna

patterns that have selected relationships with one another. For example, in a preferred embodiment, the antenna patterns at the transmitter may be constrained to be orthogonal to one another. Thus, by specifying a first antenna pattern, any remaining patterns at the base may be calculated, at least partially, according to the constraint relationships. Therefore, in a transmitter that transmits two data streams, if a first antenna pattern is specified, the antenna pattern for the second data stream may be derived, or calculated, so that the second pattern is constrained to be orthogonal to (or have low correlation with) the first.

Details on V Quantization

The simplest method of quantizing a matrix is to quantize each element of the matrix individually. Unfortunately, this method is inefficient and will require the greatest number of feedback bits for a desired performance. V may be quantized with two basic approaches: "block" and "incremental" quantization. In the first approach, all columns of V are quantized at once. In the second approach, columns of V are quantized incrementally.

Block V Quantization

Because the **V** matrix is orthonormal, it has some structure that can be exploited to reduce the amount of feedback. For the 2-antenna transmitter and 2-antenna receiver case, the **V** matrix can be written as

$$\mathbf{V} = \begin{bmatrix} v_{11} & v_{12} \\ v_{21} & v_{22} \end{bmatrix} = \begin{bmatrix} \cos\alpha & \sin\alpha \\ e^{j\theta} \cdot \sin\alpha & -e^{j\theta} \cdot \cos\alpha \end{bmatrix},$$

where

$$\alpha = \cos^{-1}(v_{11}),$$
$$\theta = \angle v_{21}.$$

The entire **V** matrix can be represented by two real parameters. Using this representation, there is a sign ambiguity in the second column vector that must be handled at the receiver. Fortunately, the transmission remains orthogonal and an MMSE receiver handles the sign ambiguity automatically. The parameters $\alpha \in \left[0, \frac{\pi}{2}\right]$ and $\theta \in [0, 2\pi]$ are uniformly quantized to a desired level. Figure 5 shows that quantizing **V** with 5 bits (3 for θ, 2 for α) and using an MMSE receiver is within 0.4 dB of the unquantized case.

In general, a codebook of **V** matrices can be created and indexed. A technique such as vector quantization can be used to generate the codebook and also to create an efficient mapping between **V** and the codebook. Parametric quantization as used in the 2x2 case can also be extended to larger **V** matrices.

Incremental V Quantization

In this approach, the columns of V are repeatedly drawn from a codebook of antenna array weights. (For example, one may use the TX AA codebooks from the 3GPP standard, release 99, or extensions of these codebooks.) The correlation properties of the columns of V are mirrored by selecting successive antenna array weight sets from increasingly smaller subsets of the codebook. As will be shown below, this constrained search reduces the amount of feedback data.

The column of V corresponding to the highest quality stream is selected first. This column is selected as the antenna array weight set that produces the maximum power at the receiver. The entire codebook is searched for this weight set.

Next, a second column of V is selected. A subset of the antenna array codebook may be found by searching for a codebook entries that have a correlation below a desired correlation threshold. The correlation threshold may be set to zero to select an orthogonal subset. Then, the antenna array weight set that produces maximum power at the receiver is selected from the low correlation subset of the codebook.

If there are three data streams, the third column of **V** is selected from a subset of the subset of codebook entries that was searched for the second column of **V**. The subset contains antenna array weight sets with low correlation against the subset searched for the second column. This process continues for all streams.

Since successive columns of **V** are searched from successively smaller subsets of the antenna array codebook, successive columns of **V** can be represented with fewer feedback bits. In a 4-element antenna array codebook with 64 entries, the antenna array weight set for the first column of **V** can be represented with log2(64) = 6 bits. By selecting an appropriate correlation threshold, the second column of **V**'s weight set can be represented with 4 bits, a third column with 2 bits, and the fourth column with 0 bits (only 1 antenna array weight set is possible, given the correlation threshold constraint and the choice of the other 3 antenna array weight sets.) Therefore, the entire **V** matrix can be quantized with 12 bits.

The size of codebook subsets may not be integer powers of two (since their size is determined by the correlation threshold), which means that the successively computed weight sets are not efficiently quantized using an integer number of bits to separately represent each weight set. In this case, alternate embodiments may jointly code the weight sets using vector quantization, or use variable length code words to reduce the number of bits required to represent the entire **V** matrix. Note that these alternate embodiments still draw the antenna array weight sets from subsets of a single codebook of antenna array weight sets, with the difference being the source coding used to reduce the number of bits required to represent the **V** matrix.

In addition to feeding back selected antenna array weight sets, the receiver may also feedback data that allows the transmitter to select a forward error correction coding scheme, a modulation scheme, a power allocation for each data stream, and a selection of antennas in the transmit antenna array.

As shown in block **308,** the process may select a data rate for each data stream in response to the composite channel measurement, the selected antenna array weight set, and SNR for each data stream. In a preferred embodiment, the SNR for each data stream is used to lookup a combination of encoding and modulation techniques according to calculated performance curves, and assuming equal power is available for both data stream. This lookup will provide an aggregated data throughput. This throughput value is compared to a second lookup assuming that all the power is used in the data stream having the highest signal to noise ratio. The second lookup gives a second data throughput, and the encoding and modulation scheme at the particular power setting is selected based upon the maximum throughput.

In a preferred embodiment, the codebook shown in table 1 below may be used in a system that sends four bits of feedback from the receiver to the transmitter in order to specify modulation and error encoding schemes for each data stream, and power allocation for each data stream. Note that antenna array weight sets are not included in the codebook of table 1.

Configuration #	Modulator #1	Code #1	Modulator #2	Code #2	Power 1	Power 2
1	QPSK	R=1/2	----	R=1/2	1	0
2	QSPK	R=1/2	QPSK	R=1/2	0.5	0.5
3	16 QAM	R=1/2	----	R=1/2	1	0
4	16 QAM	R=1/2	QPSK	R=1/2	0.5	0.5
5	16 QAM	R=1/2	16 QAM	R=1/2	0.5	0.5
6	64 QAM	R=1/2	----	R=1/2	1	0
7	64 QAM	R=1/2	QPSK	R=1/2	0.5	0.5
8	64 QAM	R=1/2	16 QAM	R=1/2	0.5	0.5
9	64 QAM	R=1/2	64 QAM	R=1/2	0.5	0.5
10	256 QAM	R=1/2	----	R=1/2	1	0
11	256 QAM	R=1/2	QPSK	R=1/2	0.5	0.5
12	256 QAM	R=1/2	16 QAM	R=1/2	0.5	0.5
13	256 QAM	R=1/2	64 QAM	R=1/2	0.5	0.5
14	256 QAM	R=1/2	256 QAM	R=1/2	0.5	0.5

Table 1

After the data rate is selected, the process transmits the selected data rate to the transmitter so the transmitter can select data encoding and modulation schemes for each data stream, as illustrated at block **310**. In a preferred embodiment of the invention, the receiver computes data rates, encoding schemes, modulation schemes, and power levels for each data stream, and transmits data that indicates these selections to the transmitter. In an alternative embodiment, the receiver may transmit measurements, or data based upon measurements, to the transmitter so that the transmitter may select a data rate, an encoding scheme, a modulation scheme, and a power allocation for each data stream.

Once the feedback data is transmitted from the receiver to the transmitter, the process ends, as depicted at block **312**. Although an end to the receiver feedback process is shown at block **312**, the process may iteratively continue in the receiver, beginning again at block **302** with new composite channel measurements.

With reference now to **FIG. 7**, there is depicted a high-level logic flow chart that illustrates a feedback method in a multiple-stream, multiple-antenna transmitter in accordance with the method and system of the present invention. As illustrated, the process begins at block **400**, and thereafter passes to block **402** wherein the process transmits a pilot signal on each antenna of the antenna array. Each pilot signal is distinguishable from the others. For example, different spreading codes may be used, or the same spreading code may be shifted in time relative to the other array antennas. These pilot signals provide a reference signal for the composite channel measurement.

Next, the process receives indications of a selected array weight set, with one set per data stream, as illustrated at block **404**. The indications of selected array weight sets may be data that describe a set of gains and phases for antenna signals for each antenna, with a set for each data stream in the transmitter. In a preferred embodiment, the selected array weight sets used for each data stream may be specified through the use of a codebook value received from the receiver, wherein the codebook value is used to lookup preselected sets of array weights.

Similarly, the process receives data that indicates data rates for each data stream, as depicted at block **406**. By indicating the data rate for each stream, the feedback data may also be indicating an encoding scheme, and a modulation scheme. The relationship

between data rates and encoding and modulation schemes exists because different encoding and modulation schemes have different capacities. Therefore, the selection of a data rate may force the selection of particular encoding and modulation schemes.

Next, the process receives an indication of power allocation for each data stream, as illustrated at block **408**. Note that a codebook value may be used as the "indicator" that indicates data rates and power allocation for each data stream. As discussed above, a single codebook value may be used to specify an encoding scheme, a modulation scheme, and a power allocation. In some embodiments, specifying a data rate alone may specify the encoder, modulator, and power allocation. For example, if the data rate selected was zero, no power is allocated and the encoding and modulation schemes are irrelevant.

After receiving the feedback data, the process selects power settings, and encoding and modulation schemes for each data stream, as depicted at block **410**. In this step, these parameters may be selected according to a codebook value received. In alternative embodiments, some of these parameters may be calculated or derived from the feedback data received. For example, if the antenna pattern of the first data stream is indicated, the process in the transmitter may derive or calculate an antenna pattern used for the second data stream. This may be done when, for example, the second stream is constrained to be orthogonal to the first stream.

Once transmit parameters are selected as shown in block **410**, the process separates input data into data streams according to selected data rates supported by encoding and modulation schemes selected for each data stream, as depicted at block **412**. This process is implemented in data splitting function **28** shown in **FIG. 3**. As an

example, if data stream 1 operates at twice the rate of data stream 2, then two symbols are sent to data stream 1 and a single symbol is sent to data stream 2. Similarly, if one data stream has zero power allocated, all the data symbols are sent to the remaining data streams having some power allocated.

Next, the process encodes each data stream, as illustrated at block **414**. The process of encoding may be implemented with a block coder, a convolutional coder, a turbo coder, and the like.

After encoding, each data stream is modulated, as depicted at block **416**. This modulation may be implemented using a BPSK modulator, a QPSK modulator, a M-PSK modulator, a M-QUAM modulator (where M is the number of constellation points), and the like.

Following the modulating step, the process modifies the gain and phase of each modulated data stream according to respective selected array weight sets to produce data stream antenna signals for each array antenna, as illustrated at block **418**. Examples of data stream antenna signals are the outputs of phase shifters **82** in **Fig. 4**. The number of data stream antenna signals produced in this step equals the number of data streams times the number of antenna elements in the antenna array.

After producing data stream antenna signals for each array antenna, the data stream antenna signals associated with the same array antenna are summed to produce antenna signals, as depicted at block **420**. Examples of antenna signals are the outputs of summers **84** in **Fig. 4**. These antenna signals are combinations of signals from each data stream that have been weighted in gain and phase according to the selected array weight sets. This complex combination

of signals is more concisely described according to the **V** matrix used in the transmitter, which is discussed above in relation to **FIG. 1**.

Finally, the antenna signals for each antenna are transmitted, as illustrated at block **420**. The transmission step includes further processing, upconversion, and amplification needed for radio frequency transmission.

The feedback method ends, as depicted at block **424**. Although the process is shown with an end, the process may iteratively repeat in the transmitter in order to update each antenna pattern for each data stream in response to varying channel conditions.

Turning now to **FIG. 8**, there is depicted a more detailed logical flow chart that illustrates the process for estimating a composite channel and selecting array weight sets, which is shown at a higher level in **FIG. 6**. As illustrated, the process begins at block **500**, and thereafter passes to block **502** wherein the process estimates channel matrix **H** using received pilot signals, wherein a pilot signal is transmitted from each transmitter antenna. Pilots may or may not be orthogonal, but they are selected so that they are distinguishable at the receiver.

Next, the process computes a singular valve decomposition of matrix **H** to find matrix **V**, wherein $\mathbf{H} = \mathbf{U}\mathbf{S}\hat{\mathbf{V}}^{T}$, as depicted at block **504**. Transmitting with this **V** matrix allows operation of the MIMO channel at near Shannon capacity for MIMO.

Thereafter, the process selects an index for a quantized **V** matrix, as illustrated at block **506**. The quantizing may be preformed by a codebook lookup, or other methods, discussed above. Note that

the quantized **V** matrix represents selected antenna array weight sets. Antenna array weight sets may be quantized as a group, or separately.

After quantizing, the process estimates a signal-to-noise ratio (SNR) of each data stream based on the transmitter using the quantized **V** matrix, and assuming equal power streams, as depicted at block **508**.

Next, the process uses the estimated SNR to determine power allocation of each data stream using a waterfilling algorithm, as illustrated at block **510**. An alternative to waterfilling is a brute-force search of all quantized possibilities. In a preferred embodiment, this parameter can be quantized to a low number of bits. For example, a reasonable choice for power allocation may be one-bit indicator for both streams "on", or only one stream "on" and the other "off".

Based on the power allocation for each stream, and the estimated SNR for each stream, the process next selects the coding method and modulation method, as depicted at block **512**. This may be implemented with a lookup that maps every SNR range to a modulator-encoder combination. In general, the coding and modulating is adapted for each data stream according to the channel quality. For example, if high channel quality is indicated by a high SNR, the modulator may be set to 16-QAM; otherwise, QPSK modulation may be selected.

Finally, the process transmits, to the transmitter, indicators for a quantized **V** matrix, a power allocation for each stream, and coding and modulation methods, as illustrated at block **514**. In a preferred embodiment, the process uses a codebook to indicate quantized antenna array weight sets, and other modulation parameters.

As depicted, the process ends at block **516**.

Referring again to **FIG. 3**, the number of antennas used by transmitter **20** is equal to the number of outputs from antenna array signal processor **58**. As shown in **FIG. 3**, antenna array signal processor **58** has two outputs, output signals **62** and **64**.

As mentioned earlier, output signals **62** and **64** may be transmitted from two antennas, or multiplexer **66** may be used to select two antennas to form an antenna array from a larger number of "available antennas", such as the four antenna elements **26** shown in antenna array **24**. Thus, in some embodiments of the present invention, there exists a set of available antenna elements, from which a subset of the "available antenna elements," from which a subset of the available antenna elements may be selected to form "an antenna array", wherein the antenna array comprises antenna elements actually used to transmit the multiple data streams.

While the embodiment in **FIG. 3** shows multiplexer **66** for selecting antennas, alternative embodiments may use the **V** matrix to select antennas mathematically by multiplying signals by zero, or non-zero values according to the matrix elements.

In order to select the antenna elements from the set of available antenna elements, receiver **98** measures a composite channel that includes all channels between all pair-wise selections of all available antenna elements and all antenna elements at the receiver. Thus, in **FIGS. 3** and **5**, between transmitter **20** with 4 available antennas and receiver **98** with 2 receive antennas, the composite channel measurement forms a composite channel matrix **H** that is four rows by two columns.

At the transmitter, there are 6 ways to choose 2 antennas from a set of 4 available antennas. The antenna array is formed with the pair that yields the highest capacity composite channel. The selection process may be described by the following expression:

$$\max_i \det\left(\mathbf{I} + \frac{1}{2\sigma^2}\mathbf{H}_i'\mathbf{H}_i\right) \tag{10}$$

where (without using waterfilling) half power is allocated to each data stream, σ^2 is the noise variance, $\mathbf{I}$ is the 2x2 identity matrix, and

$$\mathbf{H}_1 = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix}, \mathbf{H}_2 = \begin{bmatrix} h_{11} & h_{13} \\ h_{21} & h_{23} \end{bmatrix}, \mathbf{H}_3 = \begin{bmatrix} h_{11} & h_{14} \\ h_{21} & h_{24} \end{bmatrix},$$
$$\mathbf{H}_4 = \begin{bmatrix} h_{12} & h_{13} \\ h_{22} & h_{23} \end{bmatrix}, \mathbf{H}_5 = \begin{bmatrix} h_{12} & h_{14} \\ h_{22} & h_{24} \end{bmatrix}, \mathbf{H}_6 = \begin{bmatrix} h_{13} & h_{14} \\ h_{23} & h_{24} \end{bmatrix}.$$

To select one of the six pairs, three feedback bits are required. In order to reduce the feedback data even more, two bits can be used to select one of four pairs.

The receiver next considers all two-by-two combinations of transmit and receive antennas, wherein there are six possible combinations of two transmit antennas and two receive antennas. For each of the six combinations, an aggregate data rate is computed, wherein the aggregate data rate is the total data rate provided by adding the data rate of data stream 1 and the data rate of data stream 2. By ranking the aggregate data rates, the antenna combination that supports the highest data rate may be selected.

In an alternative embodiment of transmitter **20**, antenna array signal processor **58** may use a **V** matrix that produces four outputs to drive four antennas in an antenna array. However, the amount of feedback data necessary to support selection of antenna array weight

sets for a four-output **V** matrix begins to consume an unacceptable percentage of capacity of the link used for feedback data. Therefore, a two-output **V** matrix is used to drive two antennas that are selected from an available set of four antennas. The two antennas that are selected support the highest aggregate data rate between transmitter **20** and receiver **98**. In the transmitter that selects antenna elements from a larger set of available antenna elements a trade-off has been made between reducing uplink feedback data and reducing downlink performance.

It should be appreciated from the discussion above that the present invention makes it possible to increase a data rate between a transmitter and receiver using a multiple-input multiple-output radio frequency channel. The feedback method disclosed is a practical solution to controlling a MIMO transceiver.

Advantages of using the MIMO radio frequency channel include the ability to double an effective data throughput without using additional communication resources, such as spreading codes, power, and bandwidth, and without employing higher order modulators. In other words, using the same communication resources, with the same modulator, the throughput can be doubled by effectively controlling the MIMO radio frequency channel. This effective control of the channel involves transmitting multiple data streams in a way that they can be separated from one another at the receiver. This MIMO channel control exploits specific knowledge of the channel gained by measuring a composite channel between the transmitter and receiver. Furthermore, proper control of the MIMO channel enables the use of linear receivers, rather than the more complex or expensive non-linear receiver. By transmitting the signal vector **x** along the channel eigenmodes (i.e., transmitting $\mathbf{z}=\mathbf{V}\mathbf{x}$ rather than **x**), we can completely separate the two streams without using non-linear detectors. Thus,

with the proper control of the MIMO channel, the non-linear receiver has no substantial advantage over the linear receiver.

Fig. 9 shows simulation results comparing quantized MIMO feedback with un-quantized, ideal MIMO feedback. There is little degradation due to quantizing.

Fig. 10 shows simulation results for a MIMO transceiver system described above. The codebook used for this simulation is found in Table 1. The **V** matrix is selected with 5 feedback bits, and the encoding, modulation, and power allocation are selected with 4 feedback bits. The simulation results show that a MIMO system with 9 bits of feedback performs about 4 dB from the theoretical MIMO Shannon bound. Note that if some combinations of modulator, coder, and power allocation occur infrequently, they can be removed with a small loss in performance, which further reduces the feedback bits needed.

The foregoing description of a preferred embodiment of the invention has been presented for the purpose of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Obvious modifications or variations are possible in light of the above teachings. The embodiment was chosen and described to provide the best illustration of the principles of the invention and its practical application, and to enable one of ordinary skill in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.

Claims

What is claimed is:

1. A feedback method in a multiple-stream, multiple-antenna receiver, the method comprising the steps of:

measuring a composite channel between a multiple-antenna transmitter and a multiple-antenna receiver to produce a composite channel measurement;

selecting a plurality of antenna array weight sets for use in the multiple-antenna transmitter in response to the composite channel measurement, wherein each antenna array weight set is associated with one of multiple data streams; and

transmitting information describing the plurality of antenna array weight sets for use in the multiple-antenna transmitter.

2. The feedback method of claim **1,** wherein the step of selecting a plurality of antenna array weight sets further includes selecting a plurality of antenna array weight sets having a cross correlation less than the inverse of a number of antenna elements in the antenna array of the multiple-antenna transmitter.

3. The feedback method of claim **1** further including the steps of:

selecting a data rate for each data stream in response to the composite channel measurement; and

transmitting information describing the data rate selection for use in the multiple-antenna transmitter.

4. The feedback method of claim **1** further including the steps of transmitting information used to describe a quality of each data stream for use in the multi-antenna transmitter.

5. The feedback method of claim **1** wherein the step of selecting the plurality of antenna array weight sets further includes the steps of:

selecting a first antenna array weight set from a codebook having a plurality of preselected antenna array weight sets; and

selecting a second antenna array weight set from a subset of the codebook.

6. The feedback method of claim **1** further including the steps of:

measuring a composite channel between a multiple-antenna transmitter and a multiple-antenna receiver to produce a composite channel measurement, wherein pilot signals are received from M number of available antennas at the multiple-antenna transmitter;

selecting N antennas to be used at the transmitter, from M number of available antennas, in response to the composite channel measurement, wherein the N selected antennas will be used to form the antenna array at the multiple-antenna transmitter.

7. A feedback method in a multiple-stream, multiple-antenna transmitter, the method comprising the steps of:

splitting user data to produce multiple data streams;

transmitting a pilot signal from each antenna of an antenna array;

receiving indications of a selected antenna array weight set for each of the multiple data streams, wherein each antenna array weight set includes weights associated with each antenna of the antenna array;

using the selected antenna array weight sets, weighting each data stream to produce antenna signals for each antenna in the antenna array; and

transmitting the antenna signals, wherein the multiple data streams are transmitted.

8. The feedback method of claim **7** further including the steps of:

encoding and modulating each of multiple data stream to produce modulated data streams; and

using the selected antenna array weight sets, weighting each modulated data stream to produce antenna signals for each antenna in the antenna array.

9. The feedback method of claim **7** further including the steps of:

receiving indications of a selected data rate for each data stream;

splitting data in proportion to the selected data rates for each data stream; and

transmitting multiple data streams using the selected data rates for each data stream.

10. The feedback method of claim **9** further including the steps of:

selecting encoding and modulation schemes for each data stream in response to the selected data rate; and

transmitting multiple data streams using the selected encoding and modulation schemes for each data stream.

5

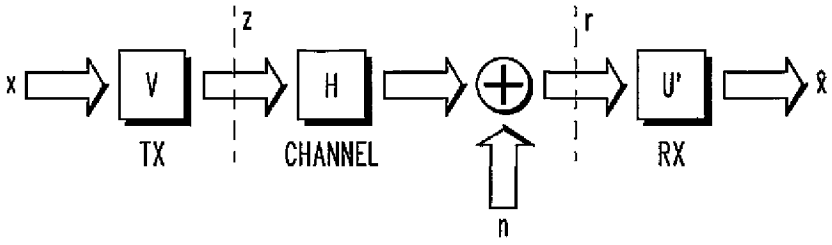

x
V
TX
z
H
CHANNEL
n
r
U'
RX
x̂

FIG. 1

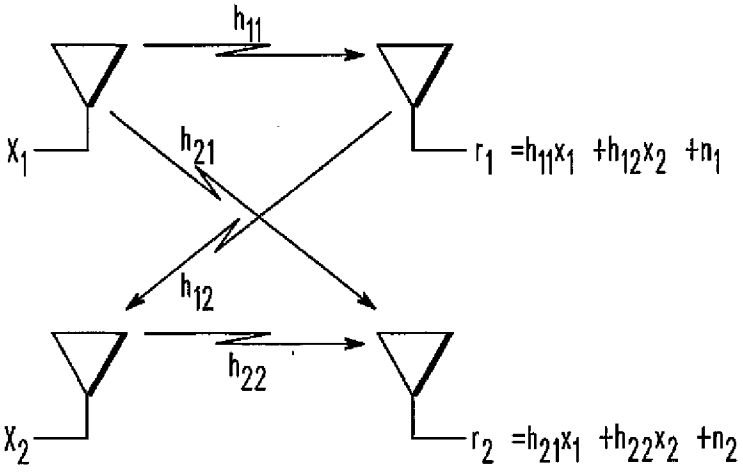

h11
X1
h21
r1 =h11x1 +h12x2 +n1
h12
h22
X2
r2 =h21x1 +h22x2 +n2

FIG. 2

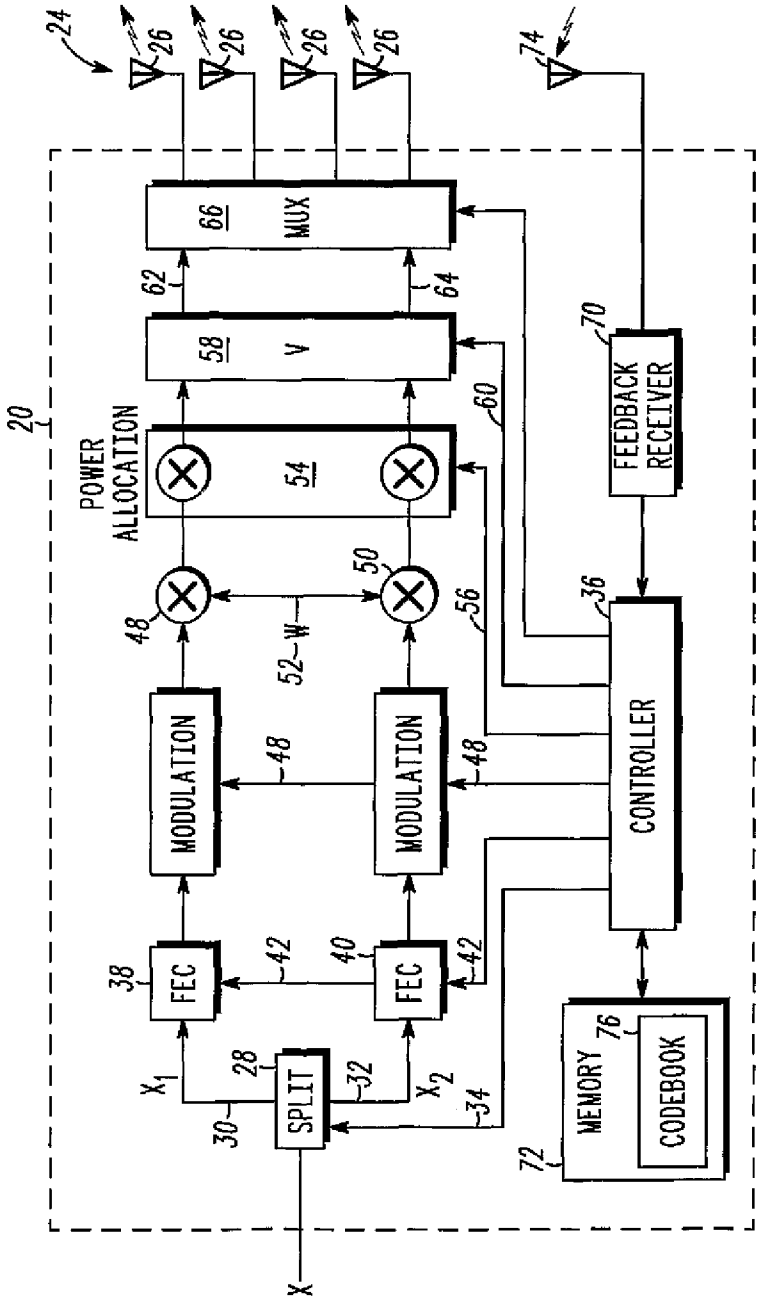

24
26
26
26
26
74
20
66 MUX
62
64
58 V
POWER ALLOCATION
54
60
70
FEEDBACK RECEIVER
48
50
52 W
56
36
MODULATION
MODULATION
48
48
CONTROLLER
38 FEC
42
40 FEC
42
X_1
28
SPLIT
32
X_2
30
34
MEMORY
76
CODEBOOK
72
X

FIG. 3

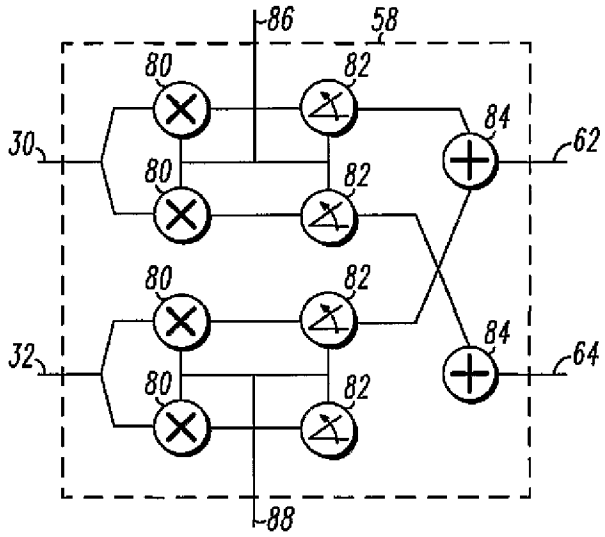


FIG. 4

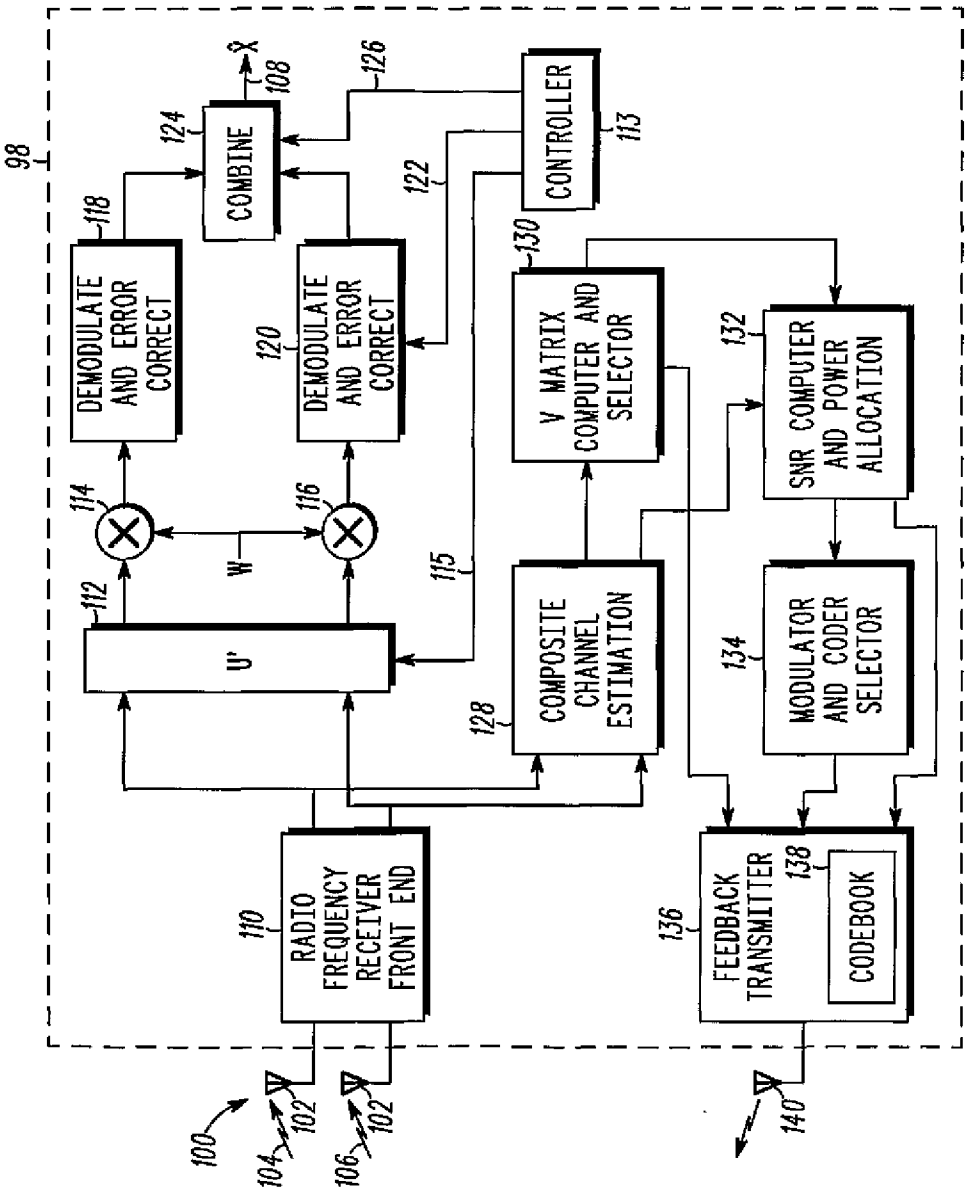

98
RADIO FREQUENCY RECEIVER FRONT END
110
U'
112
W
114
116
DEMODULATE AND ERROR CORRECT
118
DEMODULATE AND ERROR CORRECT
120
122
COMBINE
124
126
108
CONTROLLER
113
115
COMPOSITE CHANNEL ESTIMATION
128
V MATRIX COMPUTER AND SELECTOR
130
SNR COMPUTER AND POWER ALLOCATION
132
MODULATOR AND CODER SELECTOR
134
FEEDBACK TRANSMITTER
136
CODEBOOK
138
100
102
104
106
140

FIG. 5

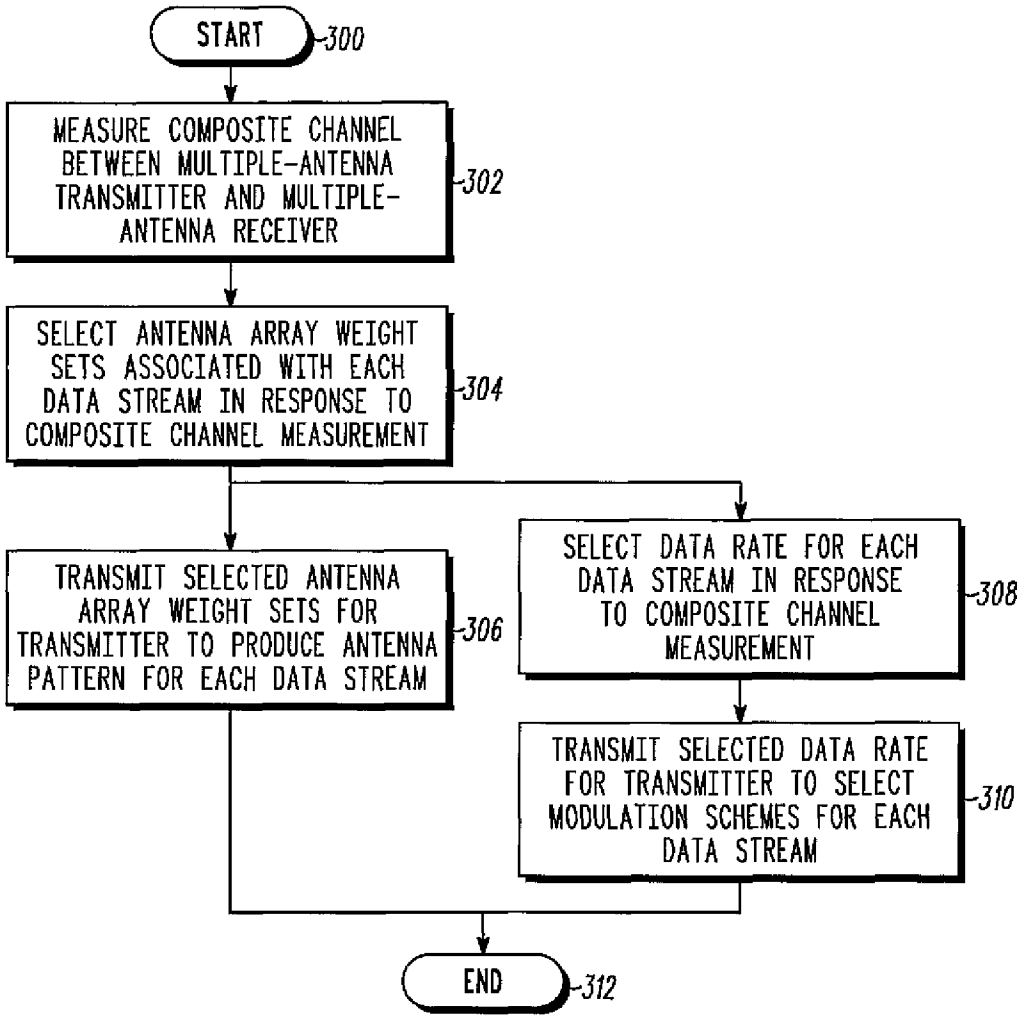

START
300
MEASURE COMPOSITE CHANNEL BETWEEN MULTIPLE-ANTENNA TRANSMITTER AND MULTIPLE-ANTENNA RECEIVER
302
SELECT ANTENNA ARRAY WEIGHT SETS ASSOCIATED WITH EACH DATA STREAM IN RESPONSE TO COMPOSITE CHANNEL MEASUREMENT
304
TRANSMIT SELECTED ANTENNA ARRAY WEIGHT SETS FOR TRANSMITTER TO PRODUCE ANTENNA PATTERN FOR EACH DATA STREAM
306
SELECT DATA RATE FOR EACH DATA STREAM IN RESPONSE TO COMPOSITE CHANNEL MEASUREMENT
308
TRANSMIT SELECTED DATA RATE FOR TRANSMITTER TO SELECT MODULATION SCHEMES FOR EACH DATA STREAM
310
END
312

FIG. 6

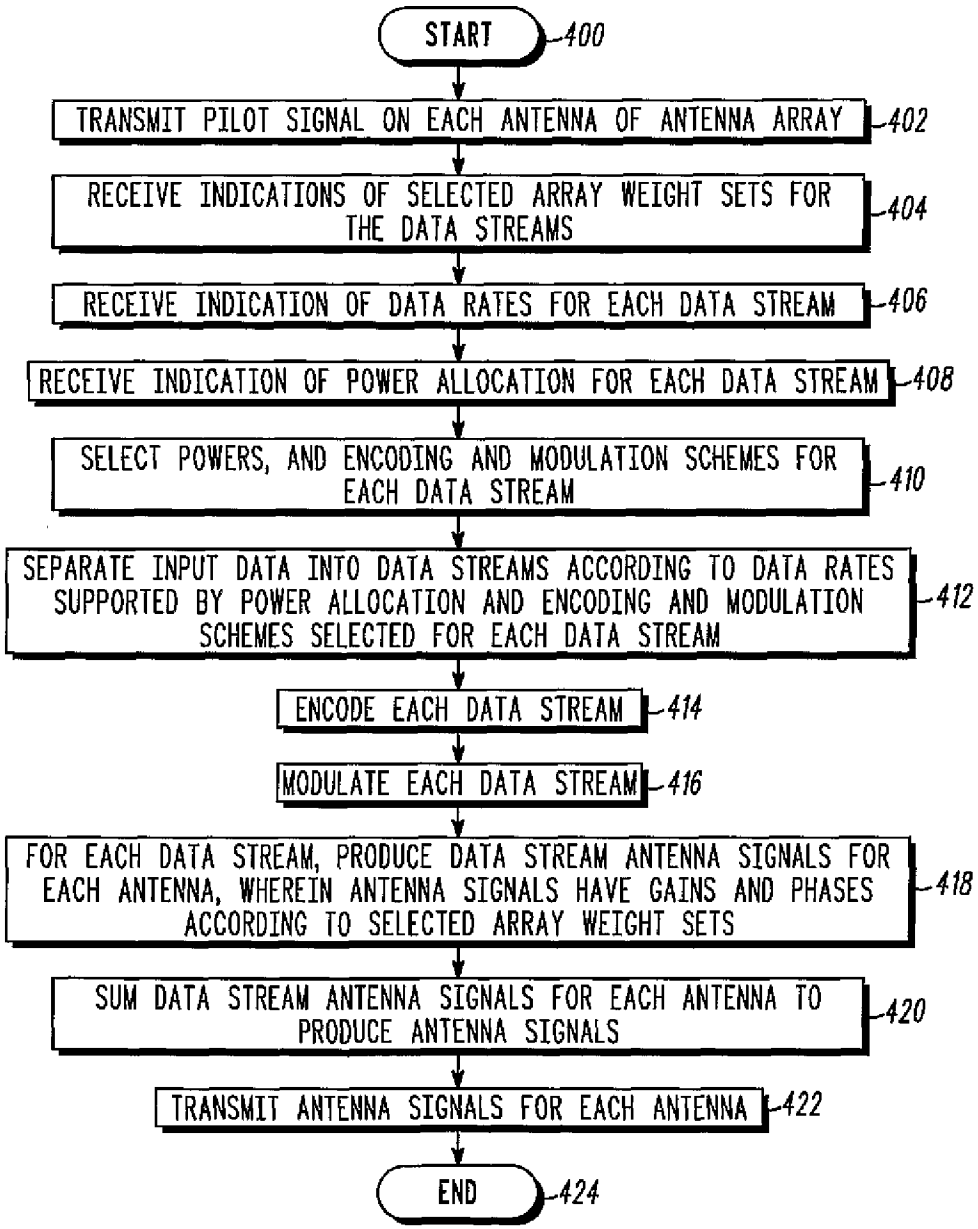

START
400
TRANSMIT PILOT SIGNAL ON EACH ANTENNA OF ANTENNA ARRAY
402
RECEIVE INDICATIONS OF SELECTED ARRAY WEIGHT SETS FOR THE DATA STREAMS
404
RECEIVE INDICATION OF DATA RATES FOR EACH DATA STREAM
406
RECEIVE INDICATION OF POWER ALLOCATION FOR EACH DATA STREAM
408
SELECT POWERS, AND ENCODING AND MODULATION SCHEMES FOR EACH DATA STREAM
410
SEPARATE INPUT DATA INTO DATA STREAMS ACCORDING TO DATA RATES SUPPORTED BY POWER ALLOCATION AND ENCODING AND MODULATION SCHEMES SELECTED FOR EACH DATA STREAM
412
ENCODE EACH DATA STREAM
414
MODULATE EACH DATA STREAM
416
FOR EACH DATA STREAM, PRODUCE DATA STREAM ANTENNA SIGNALS FOR EACH ANTENNA, WHEREIN ANTENNA SIGNALS HAVE GAINS AND PHASES ACCORDING TO SELECTED ARRAY WEIGHT SETS
418
SUM DATA STREAM ANTENNA SIGNALS FOR EACH ANTENNA TO PRODUCE ANTENNA SIGNALS
420
TRANSMIT ANTENNA SIGNALS FOR EACH ANTENNA
422
END
424

FIG. 7

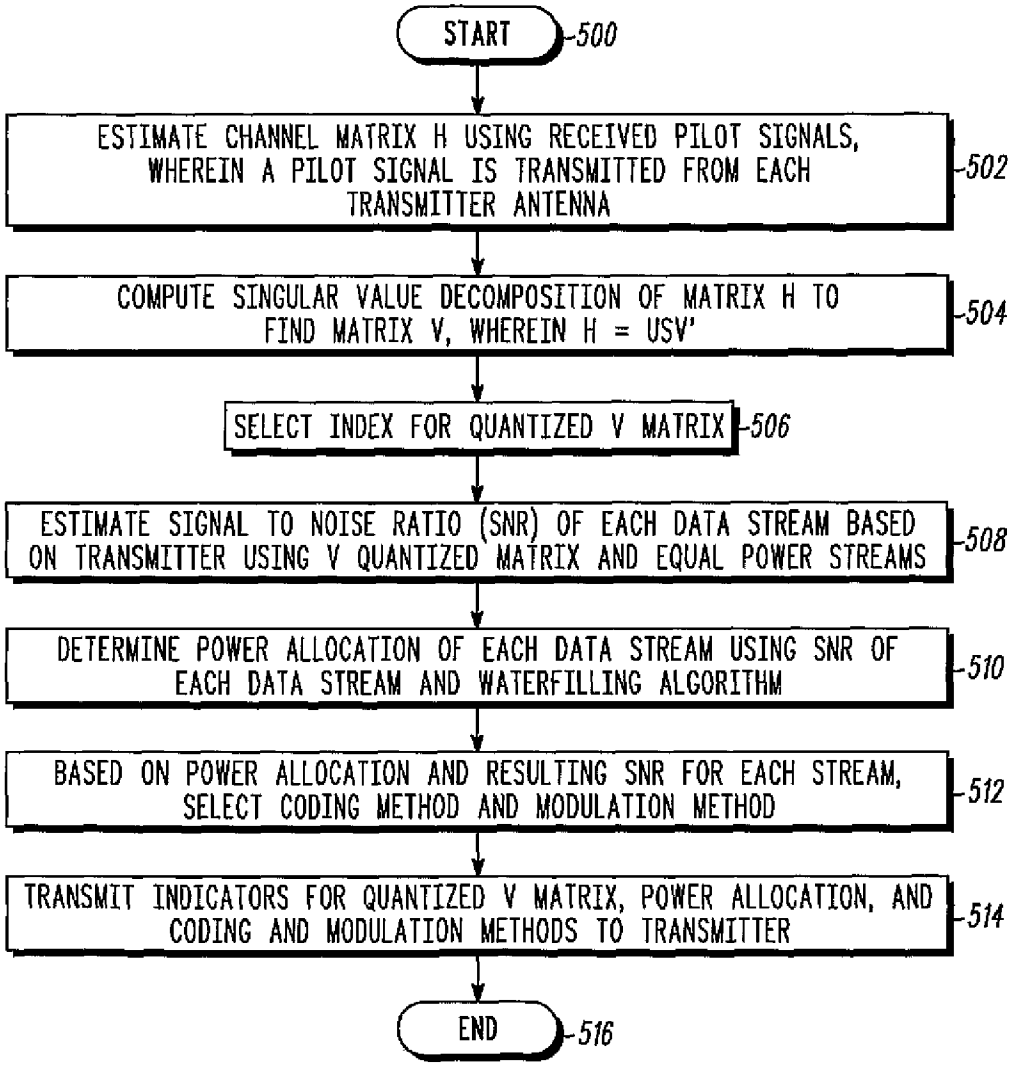

START
500
ESTIMATE CHANNEL MATRIX H USING RECEIVED PILOT SIGNALS, WHEREIN A PILOT SIGNAL IS TRANSMITTED FROM EACH TRANSMITTER ANTENNA
502
COMPUTE SINGULAR VALUE DECOMPOSITION OF MATRIX H TO FIND MATRIX V, WHEREIN H = USV'
504
SELECT INDEX FOR QUANTIZED V MATRIX
506
ESTIMATE SIGNAL TO NOISE RATIO (SNR) OF EACH DATA STREAM BASED ON TRANSMITTER USING V QUANTIZED MATRIX AND EQUAL POWER STREAMS
508
DETERMINE POWER ALLOCATION OF EACH DATA STREAM USING SNR OF EACH DATA STREAM AND WATERFILLING ALGORITHM
510
BASED ON POWER ALLOCATION AND RESULTING SNR FOR EACH STREAM, SELECT CODING METHOD AND MODULATION METHOD
512
TRANSMIT INDICATORS FOR QUANTIZED V MATRIX, POWER ALLOCATION, AND CODING AND MODULATION METHODS TO TRANSMITTER
514
END
516

FIG. 8

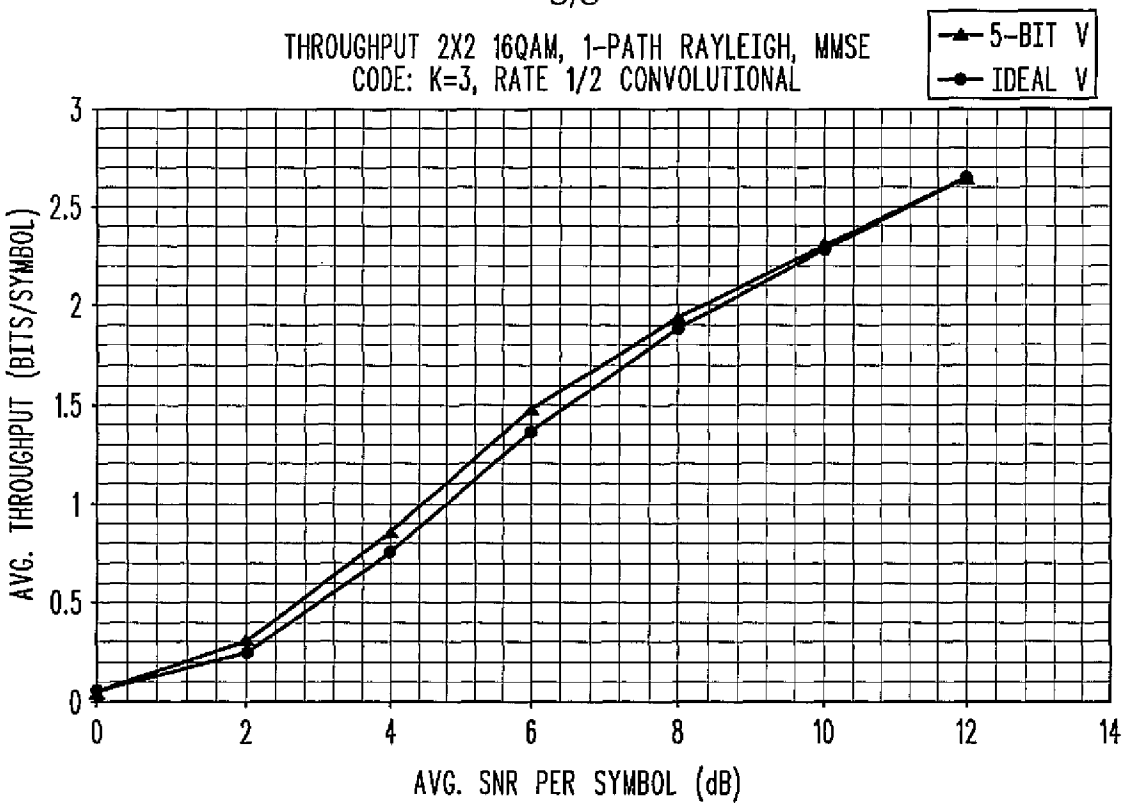
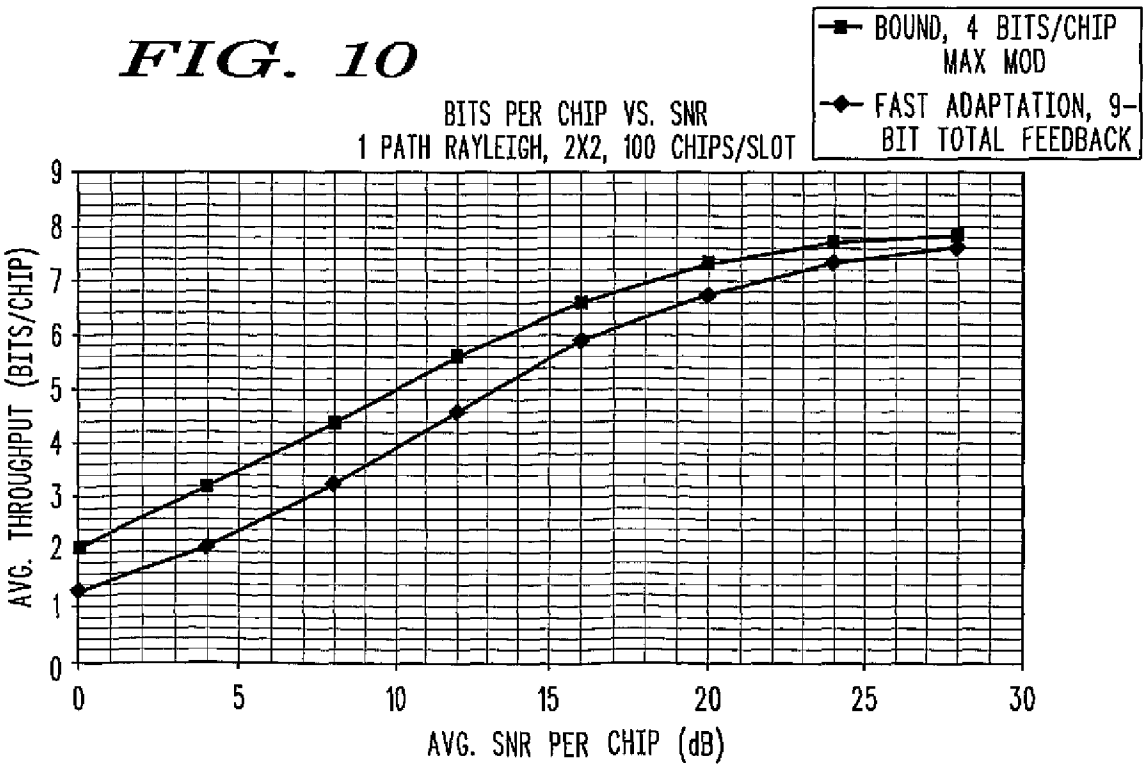

THROUGHPUT 2X2 16QAM, 1-PATH RAYLEIGH, MMSE
CODE: K=3, RATE 1/2 CONVOLUTIONAL
5-BIT V
IDEAL V
AVG. THROUGHPUT (BITS/SYMBOL)
AVG. SNR PER SYMBOL (dB)
0
0.5
1
1.5
2
2.5
3
0
2
4
6
8
10
12
14

FIG. 9

FIG. 10


BOUND, 4 BITS/CHIP MAX MOD
FAST ADAPTATION, 9-BIT TOTAL FEEDBACK
BITS PER CHIP VS. SNR
1 PATH RAYLEIGH, 2X2, 100 CHIPS/SLOT
AVG. THROUGHPUT (BITS/CHIP)
AVG. SNR PER CHIP (dB)
0
1
2
3
4
5
6
7
8
9
0
5
10
15
20
25
30

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 December 2002 (12.12.2002)

PCT

(10) International Publication Number
WO 02/099992 A1

(51) International Patent Classification[7]: H04B 1/707

(21) International Application Number: PCT/US02/18133

(22) International Filing Date: 6 June 2002 (06.06.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/296,259 6 June 2001 (06.06.2001) US
09/974,935 10 October 2001 (10.10.2001) US

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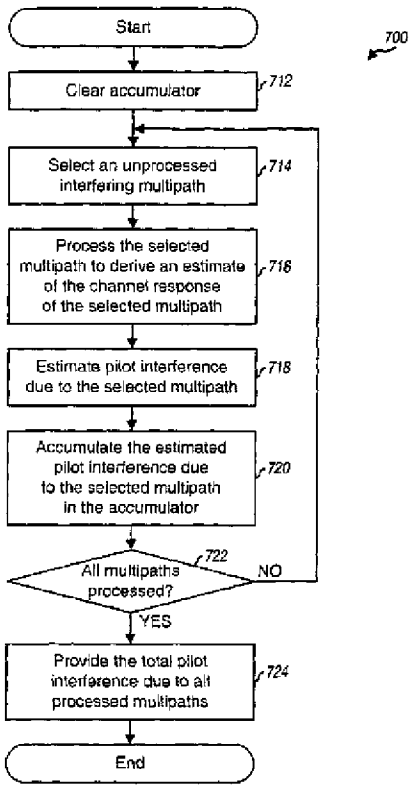
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),

[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR CANCELING PILOT INTERFERENCE IN A WIRELESS COMMUNICATION SYSTEM



(57) Abstract: Techniques for canceling pilot interference in a wireless (e.g., CDMA) communication system. In one method, a received signal comprised of a number of signal instances, each including a pilot, is initially processed to provide data samples. Each signal instance's pilot interference may be estimated by despreading the data samples with a spreading sequence for the signal instance, channelizing the despread data to provide pilot symbols, filtering the pilot symbols to estimate the channel response of the signal instance, and multiplying the estimated channel response with the spreading sequence to provide the estimated plot interference. The pilot interference estimates due to all interfering multipaths are combined to derive the total pilot interference, which is subtracted from the data samples to provide pilot-canceled data samples. These samples are then processed to derive demodulated data for each of at least one (desired) signal instance in the received signal.

WO 02/099992 A1

Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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METHOD AND APPARATUS FOR CANCELING PILOT INTERFERENCE IN A WIRELESS COMMUNICATION SYSTEM

[0001] This application claims the benefit of provisional U.S. Application Serial No. 60/296,259, entitled "METHOD AND APPARATUS FOR CANCELLATION OF MULTIPLE PILOT SIGNALS," filed June 6, 2001, which is incorporated herein by reference in its entirety for all purposes.

BACKGROUND

Field

[0002] The present invention relates generally to data communication, and more specifically to techniques for canceling interference due to pilots in a wireless (e.g., CDMA) communication system.

Background

[0003] Wireless communication systems are widely deployed to provide various types of communication such as voice, packet data, and so on. These systems may be based on code division multiple access (CDMA), time division multiple access (TDMA), or some other multiple access technique. CDMA systems may provide certain advantages over other types of systems, including increased system capacity. A CDMA system is typically designed to implement one or more standards, such as IS-95, cdma2000, IS-856, W-CDMA, and TS-CDMA standards, all of which are known in the art.

[0004] In some wireless (e.g., CDMA) communication systems, a pilot may be transmitted from a transmitter unit (e.g., a terminal) to a receiver unit (e.g., a base station) to assist the receiver unit perform a number of functions. For example, the pilot may be used at the receiver unit for synchronization with the timing and frequency of the transmitter unit, estimation of the channel response and the quality of the communication channel, coherent demodulation of data transmission, and so on. The pilot is typically generated based on a known data pattern (e.g., a sequence

of all zeros) and using a known signal processing scheme (e.g., channelized with a particular channelization code and spread with a known spreading sequence).

[0005] On the reverse link in a cdma2000 system, the spreading sequence for each terminal is generated based on (1) a complex pseudo-random noise (PN) sequence common to all terminals and (2) a scrambling sequence specific to the terminal. In this way, the pilots from different terminals may be identified by their different spreading sequences. On the forward link in cdma2000 and IS-95 systems, each base station is assigned a specific offset of the PN sequence. In this way, the pilots from different base stations may be identified by their different assigned PN offsets.

[0006] At the receiver unit, a rake receiver is often used to recover the transmitted pilot, signaling, and traffic data from all transmitter units that have established communication with the receiver unit. A signal transmitted from a particular transmitter unit may be received at the receiver unit via multiple signal paths, and each received signal instance (or multipath) of sufficient strength may be individually demodulated by the rake receiver. Each such multipath is processed in a manner complementary to that performed at the transmitter unit to recover the data and pilot received via this multipath. The recovered pilot has an amplitude and phase determined by, and indicative of, the channel response for the multipath. The pilot is typically used for coherent demodulation of various types of data transmitted along with the pilot, which are similarly distorted by the channel response. For each transmitter unit, the pilots for a number of multipaths for the transmitter unit are also used to combine demodulated symbols derived from these multipaths to obtain combined symbols having improved quality.

[0007] On the reverse link, the pilot from each transmitting terminal acts as interference to the signals from all other terminals. For each terminal, the aggregate interference due to the pilots transmitted by all other terminals may be a large percentage of the total interference experienced by this terminal. This pilot interference can degrade performance (e.g., a higher packet error rate) and further reduce the reverse link capacity.

[0008] There is therefore a need for techniques to cancel interference due to pilots in a wireless (e.g., CDMA) communication system.

SUMMARY

[0009] Aspects of the present invention provide techniques for estimating and canceling pilot interference in a wireless (e.g., CDMA) communication system. A received signal typically includes a number of signal instances (i.e., multipaths). For each multipath to be demodulated (i.e., each desired multipath), the pilots in all multipaths are interference to the data in the desired multipath. If the pilot is generated based on a known data pattern (e.g., a sequence of all zeros) and channelized with a known channelization code (e.g., a Walsh code of zero), then the pilot in an interfering multipath may be estimated as simply a spreading sequence with a phase corresponding to the arrival time of that multipath at the receiver unit. The pilot interference from each interfering multipath may be estimated based on the spreading sequence and an estimate of the channel response of that multipath (which may be estimated based on the pilot). The total pilot interference due to a number of interfering multipaths may be derived and subtracted from the received signal to provide a pilot-canceled signal having the pilot interference removed.

[0010] In one specific embodiment, a method for canceling pilot interference at a receiver unit (e.g., a base station) in a wireless (e.g., cdma2000) communication system is provided. In accordance with the method, a received signal comprised of a number of signal instances, each of which includes a pilot, is initially processed to provide data samples. The data samples are then processed to derive an estimate of the pilot interference due to each of one or more (interfering) signal instances, and the pilot interference estimates are further combined to derive the total pilot interference. The total pilot interference is then subtracted from the data samples to provide pilot-canceled data samples, which are further processed to derive demodulated data for each of at least one (desired) signal instance in the received signal.

[0011] The pilot interference due to each interfering signal instance may be estimated by (1) despread the data samples with a spreading sequence for the signal instance, (2) channelizing the despread samples with a pilot channelization code to provide pilot symbols, (3) filtering the pilot symbols to provide an estimated channel

response of the signal instance, and (4) multiplying the spreading sequence for the signal instance with the estimated channel response to provide the estimated pilot interference. The data demodulation for each desired multipath may be performed by (1) despreading the pilot-canceled data samples with the spreading sequence for the signal instance, (2) channelizing the despread samples with a data channelization code to provide data symbols, and (3) demodulating the data symbols to provide the demodulated data for the signal instance. For improved performance, the pilot estimation and cancellation may be performed at a sample rate that is higher than the PN chip rate.

[0012] Various aspects, embodiments, and features of the invention are described in further detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The features, nature, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

[0014] FIG. 1 is a diagram of a wireless communication system;

[0015] FIG. 2 is a simplified block diagram of an embodiment of a base station and a terminal;

[0016] FIG. 3 is a block diagram of an embodiment of a modulator for the reverse link in cdma2000;

[0017] FIG. 4 is a block diagram of an embodiment of a rake receiver;

[0018] FIG. 5 is a block diagram of a specific embodiment of a finger processor within the rake receiver, which is capable of estimating and canceling pilot interference in addition to performing data demodulation;

[0019] FIGS. 6A and 6B are diagrams that graphically illustrate the processing of the data samples to derive estimates of pilot interference, in accordance with a specific implementation of the invention;

[0020] FIG. 7 is a flow diagram of an embodiment of a process to derive the total pilot interference for a number of multipaths; and

[0021] FIG. 8 is a flow diagram of an embodiment of a process to data demodulate a number of multipaths with pilot interference cancellation.

DETAILED DESCRIPTION

[0022] FIG. 1 is a diagram of a wireless communication system 100 that supports a number of users and wherein various aspects and embodiments of the invention may be implemented. System 100 provides communication for a number of cells, with each cell being serviced by a corresponding base station 104. A base station is also commonly referred to as a base-station transceiver system (BTS), an access point, or a Node B. Various terminals 106 are dispersed throughout the system. Each terminal 106 may communicate with one or more base stations 104 on the forward and reverse links at any given moment, depending on whether or not the terminal is active and whether or not it is in soft handoff. The forward link (i.e., downlink) refers to transmission from the base station to the terminal, and the reverse link (i.e., uplink) refers to transmission from the terminal to the base station.

[0023] A signal transmitted from a terminal may reach a base station via one or multiple signal paths. These signal paths may include a straight path (e.g., signal path 110a) and reflected paths (e.g., signal path 110b). A reflected path is created when the transmitted signal is reflected off a reflection source and arrives at the base station via a different path than the line-of-sight path. The reflection sources are typically artifacts in the environment in which the terminal is operating (e.g., buildings, trees, or some other structures). The signal received by each antenna at the base station may thus comprise a number of signal instances (or multipaths) from one or more terminals.

[0024] In system 100, a system controller 102 (which is also often referred to as a base station controller (BSC)) couples to base stations 104, provides coordination and control for the base stations coupled to it, and further controls the routing of calls to terminals 106 via the coupled base stations. System controller 102 may further couple to a public switched telephone network (PSTN) via a mobile switching center

(MSC), and to a packet data network via a packet data serving node (PDSN), which are not shown in FIG. 1. System 100 may be designed to support one or more CDMA standards such as cdma2000, IS-95, IS-856, W-CDMA, TS-CDMA, some other CDMA standards, or a combination thereof. These CDMA standards are known in the art and incorporated herein by reference.

[0025] Various aspects and embodiments of the invention may be applied for the forward and reverse links in various wireless communication systems. For clarity, the pilot interference cancellation techniques are specifically described for the reverse link in a cdma2000 system.

[0026] FIG. 2 is a simplified block diagram of an embodiment of base station 104 and terminal 106. On the reverse link, at terminal 106, a transmit (TX) data processor 214 receives various types of "traffic" such as user-specific data from a data source 212, messages, and so on. TX data processor 214 then formats and codes the different types of traffic based on one or more coding schemes to provide coded data. Each coding scheme may include any combination of cyclic redundancy check (CRC), convolutional, Turbo, block, and other coding, or no coding at all. Interleaving is commonly applied when error correcting codes are used to combat fading. Other coding scheme may include automatic repeat request (ARQ), hybrid ARQ, and incremental redundancy repeat. Typically, different types of traffic are coded using different coding schemes. A modulator (MOD) 216 then receives pilot data and the coded data from TX data processor 214, and further processes the received data to generate modulated data.

[0027] FIG. 3 is a block diagram of an embodiment of a modulator 216a, which may be used for modulator 216 in FIG. 2. For the reverse link in cdma2000, the processing by modulator 216a includes covering the data for each of a number of code channels (e.g., traffic, sync, paging, and pilot channels) with a respective Walsh code, C_{chx}, by a multiplier 312 to channelize the user-specific data (packet data), messages (control data), and pilot data onto their respective code channels. The channelized data for each code channel may be scaled with a respective gain, G_i, by a unit 314 to control the relative transmit power of the code channels. The scaled data for all code channels for the inphase (I) path is then summed by a summer 316a to

provide I-channel data, and the scaled data for all code channels for the quadrature (Q) path is summed by a summer 316b to provide Q-channel data.

[0028] FIG. 3 also shows an embodiment of a spreading sequence generator 320 for the reverse link in cdma2000. Within generator 320, a long code generator 322 receives a long code mask assigned to the terminal and generates a long pseudo-random noise (PN) sequence with a phase determined by the long code mask. The long PN sequence is then multiplied with an I-channel PN sequence by a multiplier 326a to generate an I spreading sequence. The long PN sequence is also delayed by a delay element 324, multiplied with a Q-channel PN sequence by a multiplier 326b, decimated by a factor of two by element 328, and covered with a Walsh code (C_s = +-) and further spread with the I spreading sequence by a multiplier 330 to generate a Q spreading sequence. The I-channel and Q-channel PN sequences form the complex short PN sequence used by all terminals. The I and Q spreading sequences form the complex spreading sequence, S_k, that is specific to the terminal.

[0029] Within modulator 216a, the I-channel data and the Q-channel data ($D_{chI} + jD_{chQ}$) are spread with the I and Q spreading sequences ($S_{kI} + jS_{kQ}$), via a complex multiply operation performed by a multiplier 340, to generate I spread data and Q spread data ($D_{spI} + jD_{spQ}$). The complex despreading operation may be expressed as:

[0030]
$$\begin{aligned} D_{spI} + jD_{spQ} &= (D_{chI} + jD_{chQ}) \cdot (S_{kI} + jS_{kQ}) , \\ &= (D_{chI}S_{kI} - D_{chQ}S_{kQ}) + j(D_{chI}S_{kQ} + D_{chQ}S_{kI}) . \end{aligned} \quad \text{Eq (1)}$$

[0031] The I and Q spread data comprises the modulated data provided by modulator 216a.

[0032] The modulated data is then provided to a transmitter (TMTR) 218a and conditioned. Transmitter 218a is an embodiment of transmitter 218 in FIG. 2. The signal conditioning includes filtering the I and Q spread data with filters 352a and 352b, respectively, and upconverting the filtered I and Q data with $\cos(w_c t)$ and $\sin(w_c t)$, respectively, by multipliers 354a and 354b. The I and Q components from

multipliers 354a and 354b are then summed by a summer 356 and further amplified with a gain, G_o, by a multiplier 358 to generate a reverse link modulated signal.

[0033] Referring back to FIG. 2, the reverse link modulated signal is then transmitted via an antenna 220 and over a wireless communication link to one or more base stations.

[0034] At base station 104, the reverse link modulated signals from a number of terminals are received by each of one or more antennas 250. Multiple antennas 250 may be used to provide spatial diversity against deleterious path effect such as fading. As an example, for a base station that supports three sectors, two antennas may be used for each sector and the base station may then include six antennas. Any number of antennas may thus be employed at the base station.

[0035] Each received signal is provided to a respective receiver (RCVR) 252, which conditions (e.g., filters, amplifies, downconverts) and digitizes the received signal to provide data samples for that received signal. Each receive signal may include one or more signal instances (i.e., multipaths) for each of a number of terminals.

[0036] A demodulator (DEMOD) 254 then receives and processes the data samples for all received signals to provide recovered symbols. For cdma2000, the processing by demodulator 254 to recover a data transmission from a particular terminal includes (1) despreading the data samples with the same spreading sequence used to spread the data at the terminal, (2) channelizing the despread samples to isolate or channelize the received data and pilot onto their respective code channels, and (3) coherently demodulating the channelized data with a recovered pilot to provide demodulated data. Demodulator 254 may implement a rake receiver that can process multiple signal instances for each of a number of terminals, as described below.

[0037] A receive (RX) data processor 256 then receives and decodes the demodulated data for each terminal to recover the user-specific data and messages transmitted by the terminal on the reverse link. The processing by demodulator 254

and RX data processor 256 is complementary to that performed by modulator 214 and TX data processor 212, respectively, at the terminal.

[0038] FIG. 4 is a block diagram of an embodiment of a rake receiver 254a, which is capable of receiving and demodulating the reverse link modulated signals from a number of terminals 106. Rake receiver 254a includes one or more (L) sample buffers 408, one or more (M) finger processors 410, a searcher 412, and a symbol combiner 420. The embodiment in FIG. 4 shows all finger processor 410 coupled to the same symbol combiner 420.

[0039] Due to the multipath environment, the reverse link modulated signal transmitted from each terminal 106 may arrive at base station 104 via a number of signal paths (as shown in FIG. 1), and the received signal for each base station antenna typically comprises a combination of different instances of the reverse link modulated signal from each of a number of terminals. Each signal instance (or multipath) in a received signal is typically associated with a particular magnitude, phase, and arrival time (i.e., a time delay or time offset relative to CDMA system time). If the difference between the arrival times of the multipaths is more than one PN chip at the base station, then each received signal, $y_l(t)$, at the input to a respective receiver 252 may be expressed as:

[0040] $$y_l(t) = \sum_j \sum_i p_{i,j,l}(t) x_j(t - \hat{t}_{i,j,l}) + n(t) \quad , \qquad \text{Eq (2)}$$

[0041] where

[0042] $x_j(t)$ is the j-th reverse link modulated signal transmitted by the j-th terminal;

[0043] $\hat{t}_{i,j,l}$ is the arrival time, at the l-th antenna, of the i-th multipath relative to the time the j-th reverse link modulated signal, $x_j(t)$, is transmitted;

[0044] $p_{i,j,l}(t)$ represents the channel gain and phase for the i-th multipath for the j-th terminal at the l-th antenna, and is a function of the fading process;

[0045] $\sum_j$ is the summation for all reverse link modulated signals in the l-th received signal;

[0046] $\sum_i$ is the summation for all multipaths of each reverse link modulated signal in the l-th received signal; and

[0047] $n(t)$ represents the real-valued channel noise at RF plus internal receiver noise.

[0048] Each receiver 252 amplifies and frequency downconverts a respective received signal, $y_l(t)$, and further filters the signal with a received filter that is typically matched to the transmit filter (e.g., filter 352) used at the terminal to provide a conditioned signal. Each receiver unit 252 then digitizes the conditioned signal to provide a respective stream of data samples, which is then provided to a respective sample buffer 408.

[0049] Each sample buffer 408 stores the received data samples and further provides the proper data samples to the appropriate processing units (e.g., finger processors 410 and/or searcher 412) at the appropriate time. In one design, each buffer 408 provides the data samples to a respective set of finger processors assigned to process the multipaths in the received signal associated with the buffer. In another design, a number of buffers 408 provide data samples (e.g., in a time division multiplexed manner) to a particular finger processor that has the capability to process a number of multipaths in a time division multiplexed manner. Sample buffers 408a through 408l may also be implemented as a single buffer of the appropriate size and speed.

[0050] Searcher 412 is used to search for strong multipaths in the received signals and to provide an indication of the strength and timing of each found multipath that meets a set of criteria. The search for multipaths of a particular terminal is typically performed by correlating the data samples for each received signal with the terminal's spreading sequence, locally generated at various chip or sub-chip offsets (or phases). Due to the pseudo-random nature of the spreading

sequence, the correlation of the data samples with the spreading sequence should be low, except when the phase of the locally-generated spreading sequence is time-aligned with that of a multipath, in which case the correlation results in a high value.

[0051] For each reverse link modulated signal, $x_j(t)$, searcher 412 may provide a set of one or more time offsets, $t_{i,j,l}$, for a set of one or more multipaths found for that reverse link modulated signal (possibly along with the signal strength of each found multipath). The time offsets, $t_{i,j,l}$, provided by searcher 412 are relative to the base station timing or CDMA system time, and are related to the time offsets, $\hat{t}_{i,j,l}$, shown in equation (2) which are relative the time of signal transmission.

[0052] Searcher 412 may be designed with one or multiple searcher units, each of which may be designed to search for multipaths over a respective search window. Each search window includes a range of spreading sequence phases to be searched. The searcher units may be operated in parallel to speed up the search operation. Additionally or alternatively, searcher 412 may be operated at a high clock rate to speed up the search operation. Searcher and searching are described in further detail in U.S. Patent Nos. 5,805,648, 5,781,543, 5,764,687, and 5,644,591, all of which are incorporated herein by reference.

[0053] Each finger processor 410 may then be assigned to process a respective set of one or more multipaths of interest (e.g., multipaths of sufficient strength, as determined by controller 260 based on the signal strength information provided by searcher 412). Each finger processor 410 then receives, for each assigned multipath, the following: (1) the data samples for the received signal that includes the assigned multipath, (2) either the time offset, $t_{i,j,l}$, of the assigned multipath or a spreading sequence, $S_{i,j,l}$, with a phase corresponding to the time offset, $t_{i,j,l}$ (which may be generated by a spreading sequence generator 414), and (3) the channelization code (e.g., the Walsh code) for the code channel to be recovered. Each finger processor 410 then processes the received data samples and provides demodulated data for each assigned multipath. The processing by finger processor 410 is described in further detail below.

[0054] Symbol combiner 420 receives and combines the demodulated data (i.e., the demodulated symbols) for each terminal. In particular, symbol combiner 420 receives the demodulated symbols for all assigned multipaths for each terminal and, depending on the design of the finger processors, may time-align (or deskew) the symbols to account for differences in the time offsets for the assigned multipaths. Symbol combiner 420 then combines the time-aligned demodulated symbols for each terminal to provide recovered symbols for the terminal. Multiple symbol combiners may be provided to concurrently combine symbols for multiple terminals. The recovered symbols for each terminal are then provided to RX data processor 256 and decoded.

[0055] The processing of the multipaths may be performed based on various demodulator designs. In a first demodulator design, one finger processor is assigned to process a number of multipaths in a received signal. For this design, the data samples from the sample buffer may be processed in "segments" covering a particular time duration (i.e., a particular number of PN chips) and starting at some defined time boundaries. In a second demodulator design, multiple finger processors are assigned to process multiple multipaths in the received signal. Various aspects and embodiments of the invention are described for the first demodulator design.

[0056] The pilot interference cancellation may also be performed based on various schemes. In a first pilot interference cancellation scheme that is based on the first demodulator design, the channel response of a particular multipath is estimated based on a segment of data samples, and the estimated channel response is then used to derive an estimate of the pilot interference due to this multipath for the same segment. This scheme may provide improved pilot interference cancellation. However, this scheme also introduces additional processing delays in the data demodulation for the multipath since the segment of data samples is first processed to estimate and cancel the pilot interference before the data demodulation can proceed on the same segment.

[0057] In a second pilot interference cancellation scheme that is also based on the first demodulator design, the channel response of a particular multipath is estimated based on a segment of data samples, and the estimated channel response is

then used to derive an estimate of the pilot interference due to this multipath for the next segment. This scheme may be used to reduce (or possibly eliminate) the additional processing delays in the data demodulation resulting from the pilot interference estimation and cancellation. However, since the link conditions may continually change over time, the time delay between the current and next segments should be kept sufficiently short such that the channel response estimate for the current segment is still accurate in the next segment. For clarity, the pilot interference estimation and cancellation are described below for the second scheme.

[0058] FIG. 5 is a block diagram of a specific embodiment of a finger processor 410x, which is capable of estimating and canceling pilot interference in addition to performing the data demodulation. Finger processor 410x may be used for each finger processor 410 in rake receiver 254a shown in FIG. 4. In the following description, FIG. 5 shows the processing elements and FIGS. 6A and 6B graphically show the timing for the pilot interference estimation and cancellation.

[0059] Finger processor 410x is assigned to demodulate one or more "desired" multipaths in a particular received signal. Sample buffer 408x stores data samples for the received signal that includes the multipaths assigned to finger processor 410x. Buffer 408x then provides the appropriate data samples (in segments) to the finger processor when and as they are needed. In the embodiment shown in FIG. 5, finger processor 410x includes a resampler 522, a pilot estimator 520 (or channel estimator), a summer 542, a data demodulation unit 550, and a pilot interference estimator 530.

[0060] For each desired multipath to be demodulated by finger processor 410x, the data in all other multipaths and the pilots in all multipaths in the same received signal act as interference to this multipath. Since the pilot is generated based on a known data pattern (e.g., typically a sequence of all zeros) and processed in a known manner, the pilots in the "interfering" multipaths may be estimated and removed from the desired multipath to improve the signal quality of the data component in the desired multipath. Finger processor 410x is capable of estimating and canceling the pilot interference due to a number of multipaths found in the received signal, including the pilot of the desired multipath, as described below.

[0061] In an embodiment, the pilot interference estimation and cancellation and the data demodulation are performed in "bursts". For each burst (i.e., each processing cycle), a segment of data samples for a particular number PN chips are processed to estimate the pilot interference due to a particular multipath. In a specific embodiment, each segment comprises data samples for one symbol period, which may be 64 PN chips for cdma2000. However, other segment sizes may also be used (e.g., for data symbols of other durations), and this is within the scope of the invention. As described below, the data demodulation may be performed in parallel and in a pipelined manner with the pilot interference estimation to increase processing throughput and possibly reduce the overall processing time.

[0062] To derive an estimate of the pilot interference due to the *m*-th multipath (where $m = (i, j, l)$ and is the notation for the *i*-th multipath for the *j*-th reverse link modulated signal found in the *l*-th received signal), a segment of data samples is initially provided from buffer 408x to a resampler 522 within finger processor 410x. Resampler 522 may then perform decimation, interpolation, or a combination thereof, to provide decimated data samples at the chip rate and with the proper "fine-grain" timing phase.

[0063] FIG. 6A graphically illustrates an embodiment of the resampling performed by resampler 522. The received signal is typically oversampled at a sample rate that is multiple (e.g., 2, 4, or 8) times the chip rate to provide higher time resolution. The data samples are stored to sample buffer 408x, which thereafter provides a segment of (e.g., 512) data samples for each processing cycle. Resampler 522 then "resamples" the data samples received from buffer 408x to provide samples at the chip rate and with the proper timing phase.

[0064] As shown in FIG. 6A, if the received signal is sufficiently oversampled (e.g., at 8 times the chip rate), then the resampling for the *m*-multipath may be performed by providing every, e.g., 8-th data sample received from the buffer, with the selected data samples being the ones most closely aligned to the timing of the peak of the *m*-th multipath. The *m*-th multipath is typically a multipath assigned for data demodulation, and the multipath's time offset, t_m, may be determined and provided by searcher 412. However, pilot interference due to multipaths that are not

assigned for data demodulation may also be estimated and canceled, so long as the time offset of each such multipath is known. Each multipath's time offset, t_m, may be viewed as comprising an integer number of symbol periods and a fractional portion of a symbol period (i.e., $t_m = t_{full,m} + t_{frac,m}$) relative to the base station timing or CDMA system time, where a symbol period is determined by the length of the channelization code (e.g., 64 PN chips for cdma2000). The fractional part of the time offset, $t_{frac,m}$, may be used to select the particular segment of data samples to provide to resampler 522 and for decimation. In the example shown in FIG. 6A, the fractional part of the time offset for the *m*-th multipath is $t_{frac,m} = 5$, data sample segment 622 is provided by buffer 408x, and the decimated data samples provided by resampler 522 are represented by the shaded boxes.

[0065] For some other receiver design in which the received signal is not sufficiently oversampled, then interpolation may alternatively or additionally be performed along with decimation to derive new samples at the proper timing phase, as is known in the art.

[0066] Within pilot estimator 520, a despreader 524 receives the decimated data samples and a (complex-conjugate) spreading sequence, $S_m^*(k)$, having a phase corresponding to the time offset, t_m, of the *m*-th multipath whose pilot interference is to be estimated. The spreading sequence, $S_m^*(k)$, may be provided by spreading sequence generator 414. For the reverse link in cdma2000, the spreading sequence, $S_m^*(k)$, may be generated as shown for spreading sequence generator 320 in FIG. 3. And as shown in FIG. 6A, a segment of the spreading sequence, $S_m^*(k)$, of the same length and with the same timing phase as the data sample segment is used for the despreading (i.e., the spreading sequence, $S_m^*(k)$ is time-aligned with the decimated data samples).

[0067] Despreader 524 (which may be implemented as a complex multiplier such as multiplier 340 shown in FIG. 3) despreads the decimated data samples with the spreading sequence, $S_m^*(k)$, and provides despread samples. A pilot channelizer

526 then multiplies the despread samples with the channelization code, $C_{pilot,m}$, used for the pilot at the terminal (e.g., a Walsh code of zero for cdma2000). The decovered pilot samples are then accumulated over a particular accumulation time interval to provide pilot symbols. The accumulation time interval is typically an integer multiple of the pilot channelization code length. If the pilot data is covered with a channelization code of zero (as in cdma2000), then the multiplication with the channelization code, $C_{pilot,m}$, may be omitted and pilot channelizer 526 simply performs the accumulation of the despread samples from despreader 524. In a specific embodiment, one pilot symbol is provided for each segment, which has a size of one symbol period.

[0068] The pilot symbols from pilot channelizer 526 are then provided to a pilot filter 528 and filtered based on a particular lowpass filter response to remove noise. Pilot filter 528 may be implemented as a finite impulse response filter (FIR), an infinite impulse response (IIR) filter, or some other filter structure. Pilot filter 528 provides pilot estimates, $P_m(k)$, which are indicative of the channel response (i.e., the gain and phase, $a_m \cdot e^{j\theta_m}$) of the m-th multipath. Each pilot estimate, $P_m(k)$, is thus a complex value. The pilot estimates are provided at sufficient rate such that non-insignificant changes in the channel response of the multipath are captured and reported. In a specific embodiment, one pilot estimate is provided for each segment, which has a size of one symbol.

[0069] Pilot interference estimator 530 then estimates the pilot interference due to the m-th multipath for the next segment. To estimate the pilot interference, the pilot data and the pilot channelization code, $C_{pilot,m}$, for the m-th multipath are provided to a pilot channelizer 532, which channelizes the pilot data with the pilot channelization code to provide channelized pilot data. A spreader 534 then receives and spreads the channelized pilot data with a spreading sequence, $S_m(k+\mathrm{N})$, to generate spread pilot data (i.e., processed pilot data). The spreading sequence, $S_m(k+\mathrm{N})$, has a phase corresponding to the time offset, t_m, of the m-th interfering multipath and is further advanced by N PN chips for the next segment, as shown in FIG. 6A. If the pilot data is a sequence of all zeros and the pilot channelization code

is also a sequence of all zeros (as in cdma2000), then pilot channelizer 532 and spreader 534 may be omitted and the spread pilot data is simply the spreading sequence, $S_m(k+\mathrm{N})$.

[0070] A multiplier 536 then receives and multiplies the spread pilot data with the pilot estimates, $P_m(k)$, from pilot filter 528 to provide an estimate of the pilot interference, $I_{pilot,m}(k+\mathrm{N})$, due to the m-th multipath for the next segment. Since the pilot estimates, $P_m(k)$, are derived from the current segment and used to derive the estimated pilot interference for the next segment, prediction techniques may be used to derive pilot predictions for the next segment based on the pilot estimates. These pilot predictions may then be used to derive the estimated pilot interference for the next segment.

[0071] In an embodiment, multiplier 536 provides the estimated pilot interference due to the m-th multipath at the sample rate (e.g., 8x the chip rate) and with the timing phase of the m-th multipath. This allows the estimated pilot interferences for all multipaths (which have different time offsets that are typically not all aligned to the PN chip timing boundaries) to be accumulated at a higher time resolution. The estimated pilot interference, $I_{pilot,m}(k+\mathrm{N})$, for the m-th multipath, which includes the same number of interference samples as for the data sample segment, is then provided to an interference accumulator 538. As shown in FIG. 6A, the interference samples for the m-th multipath are stored (or accumulated with the interference samples already stored) at locations in the accumulator determined by the fractional part of the multipath's time offset.

[0072] To derive the total pilot interference for all multipaths in a given received signal, the processing described above may be iterated a number of times, one iteration or processing cycle for each interfering multipath for which the pilot interference is to be estimated and canceled from a desired multipath. The pilot interference cancellation is typically performed for the multipaths received via the same antenna, not cross antennas, because the channel estimate from one antenna is typically not good for another antenna. If the same finger processor hardware is used for multiple iterations, then the processing may be performed in bursts, with each

burst being performed on a respective segment of data samples determined by the multipath's fractional time offset.

[0073] Prior to the first iteration, accumulator 538 is cleared or reset. For each iteration, the estimated pilot interference, $I_{pilot,m}$, due to the current multipath is accumulated with the accumulated pilot interference for all prior-processed multipaths. However, as shown in FIG. 6A, the estimated pilot interference, $I_{pilot,m}$, is accumulated with samples in a specific section of accumulator 538, which is determined by the current multipath's time offset. After all interfering multipaths have been processed, the accumulated pilot interference in accumulator 538 comprises the total pilot interference, I_{pilot}, due to all processed multipaths.

[0074] FIG. 6A also shows an embodiment of accumulator 538. While finger processor 410x performs data demodulation for the m-th multipath for the current segment (using the total pilot interference, $I_{pilot}(k)$, derived earlier and stored in one section of accumulator 538), the pilot interference due to the m-th multipath, $I_{pilot,m}(k+\mathrm{N})$, for the next segment may be estimated and accumulated in another section of the accumulator.

[0075] The pilot for the m-th multipath is interference to all multipaths in the received signal, including the m-th multipath itself. For a demodulator design in which the multiple finger processors are assigned to process a number of multipaths in a received signal for a given terminal, the estimated pilot interference, $I_{pilot,m}$, due to the m-th multipath may be provided to other finger processors assigned to process other multipaths in the same received signal.

[0076] For the demodulation to recover the data on the m-th multipath, the data samples for a segment are provided from buffer 408x to resampler 522. Resampler 522 then resamples the received data samples to provide decimated data samples at the chip rate and with the proper timing phase for this multipath. The decimated data samples are processed as described above to provide the pilot estimates, $P_m(k)$.

[0077] Correspondingly, interference samples for the total pilot interference, $I_{pilot}(k)$, for the same segment are provided from accumulator 538 to a resampler 540. Resampler 540 similarly resamples the received interference samples to provide decimated interference samples at the chip rate and with the proper timing phase for the m-th multipath. Summer 542 then receives and subtracts the decimated interference samples from the decimated data samples to provide pilot-canceled data samples.

[0078] Within data demodulation unit 550, a despreader 544 receives and despreads the pilot-canceled data samples with a (complex-conjugate) spreading sequence, $S_m^*(k)$, to provide despread samples. The spreading sequence, $S_m^*(k)$, has a phase corresponding to the time offset, t_m, of the m-th multipath. A data channelizer 546 then multiplies the despread samples with the channelization code, $C_{ch,m}$, used for the code channel being recovered by the finger processor. The channelized data samples are then accumulated over the length of the channelization code, $C_{ch,m}$, to provide data symbols.

[0079] A data demodulator 548 then receives and demodulates the data symbols with the pilot estimates, $P_m(k)$, to provide demodulated symbols (i.e., demodulated data) for the m-th multipath, which are then provided to symbol combiner 420. The data demodulation and symbol combining may be achieved as described in the aforementioned U.S Patent No. 5,764,687 patent. The '687 patent describes BPSK data demodulation for IS-95 by performing dot product between the despread data and the filtered pilot. The demodulation of QPSK modulation, which is used in cdma2000 and W-CDMA, is a straight-forward extension of the techniques described in the '687 patent. That is, instead of dot product, both dot product and cross-product are used to recover the inphase and quadrature streams.

[0080] As noted above, the data demodulation for the m-th multipath may be performed in parallel and in a pipelined manner with the pilot interference estimation. While despreader 544 and data channelizer 546 are processing the pilot-canceled data samples for the current segment (with the spreading sequence, $S_m^*(k)$, and the

channelization code, $C_{ch,m}$) to provide the data symbols for the m-th multipath, despreader 524 and pilot channelizer 526 may process the same data samples for the current segment (with the spreading sequence, $S_m^*(k)$, and the pilot channelization code, $C_{pilot,m}$) to provide the pilot symbols for this multipath. The pilot symbols are filtered by pilot filter 528 to provide pilot estimates, $P_m(k)$, for the multipath. Pilot interference estimator 530 then derives the estimated pilot interference, $I_{pilot,m}(k+\mathrm{N})$, due to this multipath for the following segment, as described above. In this manner, while data demodulation is performed on the current segment using the total pilot interference, $I_{pilot}(k)$, derived from a prior segment, pilot interference for the next segment is estimated and stored to another section of the accumulator, to be used for the next segment.

[0081] In an embodiment, the pilot for a particular multipath being demodulated is estimated based on the "raw" received data samples (from sample buffer 408x) as described above, and not based on the pilot-canceled data samples (from accumulator 538). In another embodiment, the pilot may be estimated based on the pilot-canceled data samples if the total pilot interference includes some or all of the interfering pilots except for the pilot of the multipath being demodulated (i.e., the pilot of the multipath being demodulated is included in the pilot-canceled data samples). This alternative embodiment may provide an improved estimate of the channel response of the multipath being demodulated, and is especially advantageous for the reverse link where the pilot estimation is typically the limiting factor in dealing with a weak multipath. The same "other pilots canceled" data samples that is used for pilot estimation may also be processed to recover the data for the multipath, which is advantageous for a finger processor architecture that performs both pilot estimation and data demodulation in parallel on the same data sample stream. The same concept may be used to estimate the channel response of a particular interfering multipath (i.e., the estimated channel response may be based on either the raw data samples or the "other pilots canceled" data samples having interfering pilots except for the pilot of that particular multipath removed).

[0082] FIGS. 6A and 6B are diagrams that illustrate the processing of the data samples to derive estimates of pilot interference, in accordance with a specific implementation of the invention. In the example shown in FIGS. 6A and 6B, the received signal includes three multipaths that are associated with time offsets of t_1, t_2, and t_3. The received signal is digitized at a sample rate that is 8 times the chip rate to provide data samples, which are stored to the sample buffer. These multipaths may or may not be sampled at their peaks.

[0083] In the example shown in FIGS. 6A and 6B, each segment included 512 data samples for a symbol period of 64 PN chips. The pilot interference is estimated for each of the three multipaths and for each symbol period. The symbol timing for each multipath is determined by the multipath's fractional time offset. If the fractional time offsets of the multipaths are not the same, which is generally true, then the symbol timing for these multipaths will be different and will be associated with different data sample segments. In an embodiment, the multipaths are processed in an order based on their fractional time offsets, with the multipath having the smallest fractional time offset being processed first and the multipath having the largest fractional time offset being processed last. This processing order ensures that the total pilot interference is derived and available for each multipath when it is processed.

[0084] In FIG. 6A, for the n-th symbol period for the m-th multipath with a fractional time offset of $t_{frac,m} = 5$, resampler 522 receives data samples 5 through 516 from the sample buffer and provides to despreader 524 data samples 5, 13, 20, and so on, and 509, which are represented by the shaded boxes. Correspondingly, despreader 524 receives the spreading sequence, $S_m^*(k)$, with a phase corresponding to the same time offset of t_m, and despreads the decimated data samples with the spreading sequence. A pilot estimate, $P_m(k)$, is then derived based on the despread samples for this segment, as described above.

[0085] To derive the estimated pilot interference due to the m-th multipath, spreader 534 receives the spreading sequence, $S_m(k+\mathrm{N})$, corresponding to the next

segment. Multiplier 536 then multiplies the spreading sequence, $S_m(k+\mathrm{N})$, with the pilot estimate, $P_m(k)$, derived from the current segment to provide the estimated pilot interference, $I_{pilot,m}(k+\mathrm{N})$, for the next segment. The estimated pilot interference, $I_{pilot,m}(k+\mathrm{N})$, comprises interference samples 517 through 1028, which are accumulated with the samples at the same indices 517 through 1028 in the interference accumulator, as shown in FIG. 6. In this way, the fractional time offset of the m-th multipath is accounted for in the derivation of the total pilot interference.

[0086] For the data demodulation of the m-th multipath for the n-th symbol period, the same segment of interference samples 5 through 516 are provided from accumulator 538 to resampler 540. Resampler 540 then provides to summer 542 interference samples 5, 13, 20, and so on, and 509 (which are also shown by the shaded boxes), corresponding to the same-indexed data samples provided by resampler 522. The data demodulation of the pilot-canceled data samples is then performed as described above. Each multipath may be processed in similar manner. However, since each multipath may be associated with a different time offset, different decimated data and interference samples may be operated on.

[0087] FIG. 6B shows the three data sample segments, the decimated data samples, and the three spreading sequences used to derive the estimated pilot interferences due to the three multipaths.

[0088] In another demodulator design, the pilot interference estimation/cancellation and the data demodulation may be performed in real-time (e.g., as data samples are received), if sufficient processing capabilities are provided. For example, M finger processors may be assigned to concurrently process M multipaths in a received signal. For each symbol period, each finger processor can derive a pilot estimate for that symbol period, which is then used to derive the estimated pilot interference due to that finger processor's assigned multipath for the next symbol period. A summer then sums the estimated pilot interferences from all M finger processors (taken into account their respective time offsets), and the total pilot interference for the next symbol period is stored in the interference accumulator.

[0089] The total pilot interference may then be subtracted from the data samples as they are received for the next symbol period, and the same pilot-canceled data samples may be provided to all M finger processors for data demodulation. (These finger processors are also provided with the received data samples, without the pilot cancellation, which are used to derive the pilot estimates.) In this way, the data demodulation may be performed on pilot-canceled data samples in real time, and the sample buffer may possibly be eliminated. For the scheme in which the pilot estimate is used to derive the estimated pilot interference for the same segment (and not the next segment), the data samples may be temporarily stored (e.g., for one symbol period) while the total pilot interference is derived.

[0090] For the demodulator design in which the same data samples are processed multiple times (e.g., if one finger processor is assigned to process a number of multipaths), the sample buffer may be designed and operated in a manner to ensure that the data samples are not inadvertently dropped. In an embodiment, the sample buffer is designed to receive incoming data samples while providing stored data samples to the finger processor(s). This may be achieved by implementing the sample buffer in a manner such that stored data samples may be read from one part of the buffer while new data samples are written into another part of the buffer. The sample buffer may be implemented as a double buffer or multiple buffers, a multi-port buffer, a circular buffer, or some other buffer design. The interference accumulator may be implemented in similar manner as the sample buffer (e.g., as a circular buffer).

[0091] For the above demodulator design, to avoid overwriting samples that are still being processed, the capacity of the sample buffer may be selected to be at least twice the time required to derive the total pilot interference for all M multipaths (with the relationship between time and buffer capacity being defined by the sample rate). If a different data sample segment may be used for each of the M multipaths, then the capacity of the sample buffer may be selected to be at least $(2 \cdot N \cdot N_{os})$ for each received signal assigned to the sample buffer, where N is the duration of data samples used to derive the estimated pilot interference for one multipath and N_{os} is the oversampling factor for the data samples (which is defined as the ratio of the